A 500 MHz CCD SERIAL ANALOG MEMORY

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Summary

The design of a GaAs charge coupled device as a solution to transient recording of electrical signals is discussed. The requirements of Experiment 787 and others require the analysis of signals with a 250 MHz bandwidth. Some initial results of the work are presented.

Introduction

The experiments concerned all have a common denominator in that a series of decays will cause a 'pile-up' signal in the detector. It is required to analyse this signal in both the time and amplitude domains, utilizing a relatively low cost technique in order to analyse many nodes. A current estimate lies in the 50 cents to 1 dollar per pixel employed.

An approach to this problem uses a GaAs CCD which can operate at acquisition rates of <1MHz to >500MHz. The CCD acquires the transient signal at a sampling rate of 500 MHz for a given period. For example a 32 pixel CCD will acquire data for a period of time equal to $32 \times 2 \text{ nsec} = 64 \text{ nsec}$. At a convenient time later, subject to trigger validations etc., the contents of the GaAs CCD are fed to a conventional flash A/D or regular A/D and thence into the data-acquisition system.

Device

The device fabrication is described below.

Devices have been fabricated on MBE MOCVD and VPE epitaxial GaAs wafers. The MBE wafer was superior, probably due to the inclusion of an n- layer. This layer allowed a more uniform depletion to be achieved in the depletion modulated transport zone.

The device lithography was implemented using a Karl Suss MJB 3 UV 300 contact mask aligner and employed 1 micron rules using chromium masks.

The device is first delineated with an N+ etch to define suitable active regions for ohmic contacts. The ohmic contacts consist of a 12% Ge/Au at.wt., followed by a Ni and Au overlay. The ohmics were then alloyed at 450°C. The channel was defined by mesa etching.

The Schottky electrode are defined by a Ti/Pt/Au or Ti/Au metalization. These being deposited by e-beam. The lithography used various positive resists with the most successful being AZ 4110. All resists were used in conjunction with a chlorobenzene assisted lift-off. The subsequent Schottky metal lift-off for the <1 micron gaps was done using either an ultrasonic assisted acetone bath or a boiling Microstrip, the latter being greatly superior in terms of yield. For example, acetone assisted lift-off yielded less than 1% devices free of shorts, whereas microstrip assisted lift-off yielded >25% devices.

The dielectric layer that followed the Schottky metalization was fabricated with both Si_3N_4 using plasma enhanced CVD or polyimide (Du Pont Pyralin PI-2550). The Si_3N_4 system produced working devices but gave rise to surface state problems. The polyimide, cured at 180°C for two hours gave a much higher yield with considerably less process complication.

The subsequent processing of the devices requires the bi-level metal interconnect vias and second level metalizations to be defined using standard lithographic techniques. The second level metalization was defined by an Rf sputtered film of alloyed Ti-W (30% at.wt.Ti) which was subsequently masked by patterning an evaporated film of Ti-Au on this film using standard positive lithography. The sputtered Ti-W film was then suitably dry-etched using PECVE with CF_4 as the reactive gas species. The sputtered film of Ti-W ensures that the interconnect vias are suitably plated to minimize contact resistances between the upper and lower metalizations.

Figure 1 illustrates the device structure and Figure 4 is a photograph of a device.

Fig. 1. CCD Device Structure

Circuit Techniques

The device was driven by a GaAs MESFET driver circuit (Fig. 2). The quadrature was obtained by external delay lines and was chosen to be correct for quadrature at both the high input acquisition frequency and the lower output frequency.

The circuit employed is shown in Fig. 2. The operation of the device is as follows:

1) The input ohmic contact is pulsed with a negative pulse at the input acquisition frequency. In conjunction with G_1 provides a nominal input charge injection. The phase of this pulse is arranged to be in a quadrature period prior to ϕ_1 going positive.

2) The input signal - a potential - is applied to G_2 which will meter the quantity of charge to be injected under ϕ_1 . This is achieved when ϕ_1 goes to a potential that is positive w.r.t. G_2 . The input capacitance of the node is very low eg. 10^{-13}F .

3) The signal charge is then transported through the volume of the device by ϕ_1 , ϕ_2 , ϕ_3 and ϕ_4 which are in quadrature.

4) The signal charge is then available at the output ohmic where it creates a potential difference across the output capacitance of G_3 . The signal is buffered to the output system by a GaAs MESFET amplifier.

Some photographs of the outputs are shown in Fig. 3a, b, c and d. It is shown here that the output occurs 32 clock periods later for the 32 pixel device fabricated. However, due to the output circuit employed, the signal is dispersed and subject to high frequency clock interference.

* ϕ_2, ϕ_4 CIRCUITRY SAME AS ϕ_1, ϕ_3
ALL CAPACITORS 0.1 μ F CHIP CAPS

Fig. 2. CCD Driver Circuits

Conclusion

The preliminary results achieved to date are promising. Future efforts will be directed toward the improvement of both current processing and circuit techniques.

MBE 500 MHz clock

Fig. 3A. CCD Output Waveform at 500 Mhz

MBE 260 MHz clock $R_L=10K$

Fig. 3B. CCD Output Waveform at 260 Mhz

MOCVD 100 MHz clock $R_L = 1K$

Fig. 3C. CCD Output Waveform at 100 Mhz

MOCVD 100 MHz clock $R_L = 10K$

Fig. 3D. CCD Output Waveform at 260 Mhz

Fig. 4. Photograph of a 32 Pixel Device