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DEVELOPMENT OF TEST STRUCTURES FOR SILICON PARTICLE DETECTORS

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ABSTRACT

Not only for the development of a detector manufacturing process, but also for quality testing and radiation damage evaluation one needs appropriate test structures. These should be included in the wafer-scale devices. Several test structures have been studied in practice, especially the MOS capacitor and various small diodes. Also some effects from prolonged irradiation are reported.

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1. INTRODUCTION

Several manufacturers of silicon diode particle detectors have now adopted a planar process, encouraged by the good performance of the ion-implanted detectors made by Kemmer [1]. This planar process is a subset of the much more complicated Large Scale Integration (LSI) silicon technology, widely used for bipolar and MOS (Metal Oxide Semiconductor) electronic circuits. This approach has led to detectors with very low reverse current, and therefore better noise performance, and also it enables a wide variety of detector geometries. New detector applications are now explored, like the use of silicon microstrip detectors in high energy physics experiments [2]. Following the trend in the semiconductor industry, large wafers can be processed in large quantities (batches of 20-50 wafers of 3" or 4" diameter) so that large detectors (40 cm²) are available, and large area (> 1 m²) coverage can be envisaged.

2. A NEED FOR TEST STRUCTURES

There is not a unique way to make a good planar silicon diode detector. A process is designed in an empirical way, starting from previous experience and given some instrumental environment. Optimization criterion is the detector performance in terms of diode current and energy resolution. Obviously, the ultimate test structure is always the detector itself. However, there are good reasons to look for additional test structures: contamination control; quantitative measurement of the effect of varying parameters like oxidation temperature, implantation dose, etc.; and monitoring of the influence of prolonged exposure to radiation.

On the one hand, a manufacturer needs test structures to understand and improve his process, or just to make sure there is no source of contamination. On the other hand, a user may need test structures to evaluate the sensitivity of the device to radiation or other environmental conditions. Also, it may become of interest to adopt additional detector acceptance criteria, e.g. flat band voltage, interface state density, in addition to diode current and energy resolution.

In LSI processing it is customary to insert in-between the chips some "drop-in" chips, which contain the manufacturers test structures. In addition, at regular intervals one processes entire test wafers to check for contamination. In our case, given the wafer-scale aspect of most silicon particle detectors, it may be interesting to place some test structures on the detector chip itself, and some on a separate part of the wafer.

Many of the measurements discussed in this paper are done routinely in every microelectronics laboratory. In the field of nuclear particle detectors until recently one has not been much aware of details of the silicon microelectronics technology, and therefore there is an interest to present some specific examples.

3. DESIGN AND PROCESSING OF A TEST CHIP

At the outset one has to keep in mind that particle detectors are built with high resistivity silicon (1000-10000 Ωcm). Relatively little research has been done, using this material [3]. Apart from detectors, high resistivity silicon is used for high voltage rectifiers (thyristors) [4] and for deep depletion Charge Coupled Devices (CCD) [3,5]. Due to the low impurity concentration, $\lesssim 10^{12} \text{ cm}^{-3}$ very small amounts of charge have a determining influence on the device behaviour.

A test chip was designed as shown in fig. 1. It contains 6 diodes of $.25 \text{ mm}^2$ area, 5 smaller diodes, a strip structure of pitch $50 \mu\text{m}$, a MOS capacitor of $.08 \text{ mm}^2$, 3 field effect structures and resistance bars.

The processing is done, using 3 masks. The n-type wafers are cleaned and oxidized. B^+ implantation is done through the oxide, etched back to $\sim 50 \text{ nm}$. The rear side is implanted with As^+ or P^+ . After contact windows are etched, Al layers are evaporated on front and rear side. Finally, the wafer is sintered in forming gas.

In parallel, some wafers were processed which contain only an array of MOS capacitors of various sizes (1.1 mm^2 and smaller).

The results obtained with this process, in a standard LSI processing environment, are discussed in the following sections. The aim is to evaluate the usefulness of the test structures, rather than design an optimal detector process.

4. MOS TEST CAPACITOR

The MOS capacitor is the simplest test structure and still delivers extensive information. Many techniques of measurement and evaluation have been developed, as documented by Nicollian and Brews [6].

In fig. 2 a "low frequency" Quasi-static Capacitance-Voltage (QCV) measurement is compared with a high-frequency (HF, 100 kHz) curve, for the same 1.1 mm^2 capacitor on a n-type wafer with crystal orientation $\langle 100 \rangle$. The sweep rate for the QCV curve was $.05 \text{ V s}^{-1}$, and the measurement points are $.05 \text{ V}$ apart. The accumulation capacitance is practically identical in both the QCV and HF measurements: 480 pF . The oxide capacitance

$$C_{\text{ox}} = \frac{\epsilon_{\text{ox}}}{x_{\text{ox}}} = \frac{.338 \times 10^{-12}}{x_{\text{ox}} \times 10^{-7}} \text{ F cm}^{-2}$$

Using the measured capacitance, one finds for the oxide thickness $x_{\text{ox}} = 77 \text{ nm}$. By ellipsometry a value of 87 nm has been determined. Similar measurements for various wafers (table 1) generally show an agreement of better than 10%, although values from ellipsometry are systematically somewhat above those calculated from C_{ox} .

Under inversion the measured capacitance C'_{min} is the series combination of C_{ox} and the capacitance of the maximum depletion layer $C_{\text{dmin}} = \epsilon_{\text{si}}/x_{\text{dmax}}$

$$\frac{1}{C'_{\text{min}}} = \frac{1}{C_{\text{ox}}} + \frac{1}{C_{\text{dmin}}}$$

From the measured capacitance values one can calculate the effective substrate carrier concentration N_D using

$$x_{\text{dmax}} \approx 2 \sqrt{\frac{\epsilon_{\text{si}} V_T}{q N_D} \ln \frac{N_D}{n_i}}$$

where $V_T = .026 \text{ V}$, $q = 1.6 \times 10^{-19} \text{ C}$, $\epsilon_{\text{si}} = 1.054 \times 10^{-12} \text{ F cm}^{-1}$ and the intrinsic carrier concentration $n_i = 1.5 \times 10^{10} \text{ cm}^{-3}$. With the measured values $C_{\text{ox}} = 480 \text{ pF}$ and $C'_{\text{min}} = 7.8 \text{ pF}$ for 1.1 mm^2 one finds a carrier concentration $N_D = 1.5 \times 10^{12} \text{ cm}^{-3}$, corresponding to the resistivity ρ

$$\rho = \frac{1}{q \mu_e N_D} = \frac{1}{1.6 \times 10^{-19} \times 1500 \times 1.5 \times 10^{12}} = 2.8 \text{ k}\Omega\text{cm}.$$

With regard to the uncertainty on the capacitance measurement, this value is in good agreement with the nominal resistivity of the virgin silicon wafer: $1.6 \text{ k}\Omega\text{cm}$. At this point it may be noted that the depletion layer thickness $x_{\text{dmax}} \approx 15 \text{ }\mu\text{m}$ for this wafer and the Debye length L_D is $5 \text{ }\mu\text{m}$. This illustrates the unusual characteristics of the high resistivity silicon.

The depletion capacitance in the flat band condition can be expressed

$$C_F = (\sqrt{2} \epsilon_{si}) / L_D \quad \text{F cm}^{-2}$$

with

$$L_D = \sqrt{\frac{2 \epsilon_{si} V_T}{q N_D}} \quad \text{cm}$$

Using $N_D = 1.5 \times 10^{12} \text{ cm}^{-3}$, $C_{ox} = 480 \text{ pF}$ and area 1.1 mm^2 , the total capacitance C_{FB} at the flat band voltage V_{FB} is

$$\frac{1}{C_{FB}} = \frac{1}{C_{ox}} + \frac{1}{C_F}$$

and the result is $C_{FB} = 32 \text{ pF}$, corresponding (fig. 2) to a flat band voltage $V_{FB} = -0.7 \text{ V}$.

The same calculations were performed for several wafers processed in two different batches, and the results are shown in table 1.

The calculated resistivity ranges from 2.6 to 4.1 $\text{k}\Omega\text{cm}$ for the $\langle 100 \rangle$ silicon^(*) (nominal value 1.6 $\text{k}\Omega\text{cm}$), and from 3.9 to 9.3 $\text{k}\Omega\text{cm}$ for the $\langle 111 \rangle$ silicon (nominally 5 $\text{k}\Omega\text{cm}$). Two wafers show however 27 $\text{k}\Omega\text{cm}$. The flat band voltages are closer to 0 for the $\langle 100 \rangle$ substrates (-0.7 to -1.7 V) than for the $\langle 111 \rangle$ substrates (-2.1 to -5.3 V). This is also illustrated in fig. 3. The higher density of oxide charge (related to "dangling bonds") on $\langle 111 \rangle$ silicon is responsible for this difference. Further inspection of table 1 shows that all wafers processed in batch C have larger V_{FB} than those processed in batch B. The wafers with P^+ rear contact have the highest V_{FB} . The variation of V_{FB} over a single wafer is less than .3 V.

Among the numerous measurements which can be made on the MOS capacitor, the Bias Temperature Stress (BTS) and the pulsed capacitor carrier lifetime measurement are of practical interest.

After a 10 min. stress at 250°C , with $2 \times 10^6 \text{ V cm}^{-1}$ stress voltage over the oxide, our samples did not show a shift of the C-V curve under the influence of mobile oxide charge. The standard set-up for this measurement could not be used, because the capacitors did not respond to the 1 MHz measurement frequency,

(*) All silicon was supplied by Wacker-Chemitronic.

presumably due to the high substrate resistance. At 100 kHz there is hardly any difference with the capacitance value in accumulation, found in the quasi-static QCV measurement.

By observing the transient behaviour of a MOS capacitor, pulsed e.g. from flat band voltage to deep depletion, it is possible to determine the minority carrier lifetime τ_p (in n-type Si) from the time needed to return to thermal carrier equilibrium. The minority carrier response time is proportional to N_D/n_i and therefore the measurement is more difficult for a low impurity concentration N_D . Minority carrier lifetimes of 1 ms and longer are observed. It may be noted that the hole diffusion length L_p under this condition is > 1 mm.

5. DIODE REVERSE CURRENT AND BREAKDOWN

Measuring forward and reverse diode current does not present much of a problem, in principle. The diode areas were chosen .01 mm², .04 mm² and .25 mm². However, the reverse currents are so small that precise measurement may be difficult. From the values reported in fig. 4 it appears that edge current is important. Also, due to lateral extension of the depletion region the effective diode area is not well determined, which complicates exact comparisons. The typical reverse current obtained in our sample diodes is .1 nA at 100 V, for the diodes of .25 mm². This corresponds to 10-40 nA . cm⁻² or 250-1000 nA . cm⁻³, depending on the lateral extension assumed.

The lateral extension of the depletion layer also causes strong curvature in the diode capacitance-voltage curve, so that it is difficult to determine values for resistivity and total depletion voltage. Test diodes for these purposes have to be made bigger than a few mm², and will necessarily take some room on the wafer.

Breakdown characteristics may be tested with smaller structures. The influence of a floating field plate and an ion-implanted guard ring are illustrated in fig. 5. The field plate is not very effective, but the floating guard ring always improves the breakdown voltage. The breakdown is "self-healing" as is shown in fig. 6, where 3 consecutive measurements on a circular diode show a nearly 50% increase in breakdown voltage. After healing the diodes withstand 150-200 V, at .2-.4 nA, but the healing may take many hours. Also, unlike the regular "walk-out" phenomenon, the healing is reversible after the diode has been switched off for a while. Usually, this type of behaviour is explained by trapping of hot electrons in the oxide edge of the diode.

The leakage currents of diodes which have a separate bonding pad, positioned on the oxide, are always higher than those of comparable diodes without such a bonding pad. The oxides were relatively thin and they cannot sustain as high voltages as the thick silicon depletion layers. In particular, the strip diode structure showed these effects. Increasing the oxide thickness to 200 nm gave a considerable improvement for the strip diode currents, but they are still 3-5 times larger than those of the normal diodes.

The detection characteristics of the diodes are excellent as long as the reverse current is low. In fig. 7 a ^{57}Co photon spectrum is shown, with a FWHM of 3 keV of the 122 keV photoabsorption peak.

6. FIELD EFFECT STRUCTURES

Three field effect structures (FET) were included in this test chip. The aluminium gate is not overlapping with the source and drain implantations, so that these structures are different from the usual MOSFET transistors. Also, the positioning of the gate between source and drain is not symmetrical, and this is clearly seen in the difference between fig. 8(a) and 8(b).

The ratios W/L are 10, 25 and 50 for these structures, and in spite of the large channel lengths, one observes in all devices punch-through as in a VLSI short-channel device.

In fig. 9 the current in the channel is shown as a function of the gate voltage V_{GS} . The threshold voltage found here corresponds to the flat band voltage + 2 times the energy $E_F - E_i$ ($\sim .1$ V for this impurity concentration).

7. IRRADIATION TESTING

Irradiation of silicon detectors creates defects in the bulk of the silicon, in the oxide, and in the interface region. Also, free electrons and holes generated by the radiation may be trapped in places which otherwise would not be charged.

Current or capacitance measurements using a diode structure enable the study of the bulk silicon. Eventually, more detailed information about the radiation induced defects can be obtained with temperature dependent measurements like Thermally Stimulated Current (TSC) or Deep Level Transient Spectroscopy (DLTS).

The MOS capacitor again plays an eminent role in the study of the oxide and the interface charges. Under the influence of the irradiation one observes a shift of the flat band voltage (see e.g. [6], p. 559). In fig. 10 the flat band voltage shift is shown as a function of dose in a 12 keV x-ray irradiation of one of the test chips. During irradiation a reverse bias was applied to the diodes, as well as to the MOS capacitor. The shift is 81 mV per krad. "Stretch-out" of the transition from accumulation to depletion is indicative for the presence of charge non-uniformity or for an increase in interface trap density.

The behaviour of the diode reverse currents during the irradiation was found to be erratic: currents increased or decreased independently without a clear relation to the irradiation. During the test only 3 diodes could be monitored. Afterwards, several diodes on the chip were apparently connected together, although the minimum distance between elements is 300 μm . One diode which apparently has become bad, if not connected, still adds current to adjacent diodes which themselves have low current. Long surface channels are probably the cause of these interconnections. To study these phenomena in more detail, test structures with a network of field plates could be useful. Several weeks after the 10 krad irradiation the diode currents are nearly back to their original values, showing that really the oxide-silicon interface is at cause.

8. CONCLUSIONS

The MOS capacitor is a very useful test device, but it should not be too small, otherwise the displacement currents to be measured in the QCV measurement are below 1 pA. On the other hand, a too large capacitor may show pinhole short-circuits. Similarly, a test diode must be sufficiently big to eliminate the preponderance of edge effects.

The use of various test devices on a single high resistivity substrate may present a problem, especially under irradiation.

The measurement of minority carrier lifetime requires special precautions, as will also be explained elsewhere in these Proceedings by Herwijnen and ten Kate.

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TABLE I

Parameters obtained from C-V measurement on MOS capacitors

Wafer no	Crystal orientation	Capacitor area (mm ²) (nominal)	Capacitance (pF)		Oxide thickness (nm)		Carrier concentration (cm ⁻³)	Resistivity (kΩcm)	Flat band voltage (V)
			Accumulation	Inversion	Calculated	Ellipsometry			
B1	<100>	.08	42	.6	64	70	1.6 × 10 ¹²	2.6	-9
B9	<100>	1.1	480	7.8	77	87	1.5 × 10 ¹²	2.8	-7
C10	<111>	.08	14	.4	193	192	5.4 × 10 ¹¹	7.7	-4.5
C13	<100>	.08	18	.53	150	151	1.2 × 10 ¹¹	3.5	-1.3
C14	<100>	1.1	260	6.8	143	151	1.0 × 10 ¹²	4.1	-1.0
C15 P ⁺	<100>	.08	18	.58	150	152	1.5 × 10 ¹²	2.8	-1.7
C16	<100>	.08	18	.58	150	152	1.5 × 10 ¹²	2.8	-1.2
B33	<111>	.08	34	.49	80	85	9.6 × 10 ¹¹	4.3	-2.6
B34	<111>	1.1	470	5.1	79	85	4.5 × 10 ¹¹	9.3	-2.3
B35	<111>	.08	24	.51	113	118	1.1 × 10 ¹²	3.9	-2.8
B36	<111>	.08	26	.47	104	111	8.6 × 10 ¹¹	4.8	-2.1
B37	<111>	1.1	330	3.6	113	120	1.5 × 10 ¹¹	27.	-2.4
C30 P ⁺	<111>	1.1	200	3.6	186	200	1.5 × 10 ¹¹	27.	-5.0
C38	<111>	.08	14	.50	193	200	1.0 × 10 ¹²	4.1	-3.3
C39	<111>	1.1	190	4.4	196	200	3.2 × 10 ¹¹	13.	-2.8
C40	<111>	.08	14	.49	193	201	9.6 × 10 ¹¹	4.3	-3.2
C41 P ⁺	<111>	.08	14	.51	193	201	1.1 × 10 ¹¹	3.9	-5.3

Note: B, C indicate batch.

P⁺ indicates phosphorus implantation, all other wafers have As⁺.

FIGURE CAPTIONS

- Fig. 1 Metallization mask level of the test chip, showing the various test structures discussed in the text. The bonding pads are $100 \times 100 \mu\text{m}^2$, the overall size is $3.7 \times 3.7 \text{ mm}^2$.
- Fig. 2 Quasi-static C-V curves, measured going first from accumulation to inversion and then back from inversion to accumulation (a). The curves (b) represent the same measurements but at high frequency (100 kHz). The kink in the HF curve (b) at -0.3 V is an artefact. The flat band voltage V_{FB} is indicated. The crystal orientation of this wafer is $\langle 100 \rangle$.
- Fig. 3 C-V curves, taken at 100 kHz, for 1.1 mm^2 MOS capacitors on $\langle 111 \rangle$ and $\langle 100 \rangle$ oriented n-type high resistivity silicon.
- Fig. 4 The diode reverse current (at 50 V reverse bias) as a function of the nominal diode area. The open and opaque circles indicate the extreme values for measurements on several diodes.
- Fig. 5 Comparison of reverse current vs. voltage for 3 different diode structures. The diode with ion-implanted guard ring (gr) has the highest breakdown voltage, compared to the one with a floating field plate (fp). The simple square diode (sq) has the lowest current, but also the lowest breakdown.
- Fig. 6 Improvement of the breakdown voltage with time. The curves are measured consecutively as indicated (47, 48, 49) and each measurement took $\sim 2 \text{ min}$.
- Fig. 7 Spectrum of ^{57}Co source, showing the 122 keV photopeak with a FWHM of 3 keV. The small peak to the right is at 136.5 keV.
- Fig. 8 (a) $I_{\text{DS}}-V_{\text{DS}}$ characteristics of a field effect structure on the test chip. Horizontal division 2 V, vertical division .5 mA. The threshold voltage is 3.3 V. The transconductance g_m is $70 \mu\text{A/V}$.
(b) The same structure, but with polarity inversed.

FIGURE CAPTIONS (Cont'd)

Fig. 9 Channel current in the field-effect structures, as a function of gate voltage. The current is larger, the shorter the gate length L . The width W is the same for all structures, i.e. $500\text{ }\mu\text{m}$.

Fig. 10 Shift of the flat band voltage as a function of X-ray irradiation. The MOS capacitor was at -50 V during the irradiation.

Fig. 1

B9:0804 (100)

18-7-85

Fig. 2

37:0209

18-7-85

Fig. 3

Fig. 4

Fig. 5

Fig. 6

Fig. 7

Fig. 8(a)

Fig. 8(b)

Fig. 9

Fig. 10