CONSTRUCTION AND PERFORMANCE OF A 1 m² SILICON DETECTOR IN UA2

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ABSTRACT

We describe the construction, expected performance and intended operation of a one square metre silicon array, which is being constructed for the UA2 experiment at the CERN $\bar{p}p$ Collider.

*(Contribution to the 4th. European Symposium on
Semiconductor Devices, Munich, 3-5 March, 1986)*

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1. INTRODUCTION AND GENERAL DESIGN CONSIDERATIONS.

The UA2 Collaboration is at present upgrading the UA2 detector, installed at the CERN $\bar{p}p$ Collider [1,2]. One component of the upgraded detector will be a large (1 square metre) matrix of silicon counters, arranged as a cylinder of 1 metre in length and 147.5 mm in radius, around the intersection region. This paper describes the motivation for constructing the array, the status of its construction, and its expected operation.

A major aim of the UA2 upgrade is to improve the detector's electron identification capability [2]. The silicon array, which forms part of a new charged - particle tracking detector, will assist the identification of Dalitz decays, and of photon conversions in the Collider vacuum pipe and in the detector itself. The total thickness preceding the silicon array in the upgraded UA2 detector is ~ 0.01 radiation lengths (rl). Converted photons are a potential background when the conversion occurs between the $p\bar{p}$ interaction point and the silicon array. The misidentification of photon conversions as single electrons is strongly reduced by the requirement of a low ionization energy loss in the silicon array.

The practical design of the silicon array is constrained by several considerations :

- i. the need to identify photon conversions in a high multiplicity environment, over the full solid angle used for electron identification ($25^\circ < \theta < 155^\circ$ with full azimuthal coverage), with a minimum inactive area of the array and a minimum of material preceding the silicon,
- ii. the need to ensure an acceptable signal - to - noise ratio for each detector element using commercially available electronics, implying the use of high-resistivity silicon and its operation at a stable temperature,
- iii. the need for a reliable and compact design, given the space constraints (the total radial space available is 25 mm), poor accessibility, and the radiation environment of the array,

iv. reasonable construction and operating costs.

The resulting detector design is a compromise between these somewhat conflicting requirements. The array, shown in fig. 1, consists of a matrix of silicon counters mounted on a cylinder of radius 140 mm around the beam pipe. Each of 48 modules contains 9 counters, and covers an azimuthal angle of 15° and one half of the polar angular range.

All counters are subjected to stringent quality checks before insertion in the array, as discussed in Section 2. Details of the mechanical assembly and electronic readout of the array are described in section 3. Operating experience has been gained using three completed modules of the final design in the existing UA2 experiment, and this is discussed in section 4.

2. THE SILICON COUNTERS

For the complete array, 432 silicon counters as shown in fig. 2 are required. They are commercially manufactured [3] from 3-inch wafers of n-type silicon with resistivity 2 - 15 $k\Omega$ cm. The total area of each counter is 65×43 mm² and its thickness is 0.3 mm. The active area of 61×40 mm² consists of seven ion-implanted pn junctions (pads) of area 8.7×40 mm², separated by 0.1 mm wide oxide strips and with a typical intrinsic capacitance of 120 - 130 pF at full depletion voltage. All seven pads are surrounded by a common guard ring of 0.1 mm width. The surfaces are not further protected.

Each counter is glued along one side on a 7×55 mm² printed circuit board of 1 mm thickness. The pads are wire-bonded to this board and the latter is attached mechanically and electrically via contact pins to a "mother board" common to the 9 counters (see Section 3).

Following the delivery of the silicon counters from the manufacturer, a series of mechanical and electrical tests are made to ensure the suitability of each detector for use in the UA2 apparatus. A total of 143 counters were delivered, as of March 1986.

2.1 Visual Checks

An initial visual inspection is made of the aluminium contacts, of the oxide surface, and of the quality of the counter edges. This gives a reasonable assessment of the processing, handling, cutting and cleaning of the wafers. Although the quality of the junction cannot be directly ascertained, we are able in some cases to correlate the surface appearance with defects identified in subsequent tests. The thickness of each counter is measured at this stage, for use in later counter calibrations. To minimise the effects of humidity and dust, all counters are maintained in clean-room conditions, or under nitrogen flow.

More detailed investigations of the origin of defects on silicon counters giving abnormally high leakage current have been performed using a scanning electron microscope. The BACKEBIC method, described in this conference [4], has been a useful tool to localise and analyse defects.

2.2 Electrical acceptance tests

The electrical characteristics of each silicon counter are measured on the test bench described in [5]. Up to 64 counters can be operated and measured simultaneously. Measurements are made of the reverse (or leakage) current for each pad (0-5000 nA with a resolution of 2.5 nA), and of the pad capacitance (0-500 pF with a resolution of 0.5 pF). The computerised test bench automatically measures the leakage current and capacitance as a function of the bias voltage, and the stability of leakage current for each pad. These simple electrical measurements of the ion-implanted diode give useful basic information on the behavior and quality of silicon counters.

- i. The leakage current is normally the sum of the diffusion and generation current, which depends on the carrier life-time. It is normally around 70 nA per pad at full depletion (20 nA/cm^2). Defects in the junction, due to imperfections of the

processing or from native dislocations in the silicon crystal can increase the leakage current.

A criterion for the acceptance of a counter is that the leakage current is less than 250 nA for each pad of the counter, when operated at 19°C and at full depletion voltage. This is the value of the leakage current for which the typical shot noise contribution (~ 1450 electrons r.m.s.) approximates the intrinsic preamplifier noise. Fig. 3a shows the leakage current dependence on bias voltage, for all 7 pads of a counter not satisfying the above acceptance criteria. While pads 2 to 4 show the typical leakage currents of satisfactory pads, pads 5 and 6 have a high leakage current. Curves 1 and 7 show defective pads, with a breakdown of the diode junction at low depletion voltage. To verify the long-term counter behaviour, the leakage current is monitored at regular intervals during 24 - 48 hours of operation at full depletion voltage.

- ii. The counter capacitance versus bias voltage of each pad is measured in order to determine the full depletion voltage (see fig. 3b). The resistivity of the silicon crystal is calculated from the slope of a measurement of the capacitance versus $[V_{\text{Bias}}]^{-1/2}$. The measurement is sufficiently accurate to observe inhomogeneities of the silicon resistivity along the wafer diameter. Variations of $\pm 15\%$ between the centre and edge of the wafer have been measured. This value is compatible with specifications from the supplier [6].

The measured value of the full depletion voltage is used to determine the optimum operating voltage, which is slightly higher in order to maintain a stable calibration.

2.3 Results of acceptance tests.

A total of 143 counters have been tested so far. Fig. 4 gives the distribution of their full depletion voltage as measured at the centre of the wafer. The sample clearly contains two batches of wafers, one depleting at between 60 and 100 volts and the other depleting at approximately 30 volts.

Fig. 5 shows the distribution of leakage currents at full depletion. Most pads have a reverse current of between 50 and 100 nA, but 12% of the pads have leakage current measurement exceeding 250 nA. The position dependence of these "bad pads", and the probability of finding two or more "bad pads" on a given detector, is consistent with a statistical distribution of independent defects. It should be noted, however, that neighbours of a "bad pad" have an increased risk of long-term deterioration in leakage current.

3. THE DETECTOR

3.1 Mechanics

The 9 counters of each module are mounted on a fibreglass motherboard, which measures $50 \times 582 \text{ mm}^2$ and is a six-layer printed circuit board of 0.7 mm total thickness. It supports the silicon counters on one side, and the corresponding preamplifiers on the other side. Fig. 6 shows an assembled board, and fig. 1 shows its cross section. The silicon counters are held on one side by contact pins and on the other side by small spacers. Each second counter is staggered in height by 1 mm to avoid dead spaces. The 9 counters are covered by a common 0.1 mm thick fibreglass sheet and enclosed in aluminium foil to provide electrical shielding. The volume surrounding the silicon counters is flushed with nitrogen, and the preamplifiers are flushed with cool air.

Each module is slid into a polygonal container of 0.2 mm thick fibreglass. The 48 containers are mounted on a support structure consisting of 0.6 mm thick carbon fibre cylinders. For normal incidence particles, the silicon detector has an average thickness of 0.03 μm , including 0.0045 μm preceding the silicon counters.

3.2 Outline of the electronics chain

The problem of measuring small signals (of typically 3 fC charge) with a good resolution is solved in the classical way, by cascading a low noise charge-sensitive preamplifier and a shaping amplifier with an adequate shaping time constant. However, given the small volume occupied by the 3024 channels of this array, the amplifiers must be small, and operate with a low power consumption to minimise heat dissipation.

A block diagram of the electronics is given in Fig. 7. For each module the preamplifier output signals are transmitted via the multilayer motherboard to an electronics box supported outside the detector acceptance. At this stage, the pulses are shaped, and the track-and-hold and multiplexing functions are made. A multiplexed readout scheme is chosen for logistic reasons, since no fast-trigger information is required from this array.

3.3 The preamplifier hybrid circuit

We use a specially developed hybrid circuit [7] which contains 7 preamplifiers with FET-input stage, input decoupling capacitors, and individual bias voltage filters for each channel and the guard ring. A double-sided mounting technique allows for the small size of the hybrid circuit of $(30 \times 51 \text{ mm}^2)$, which fits well to the size of our silicon counters.

The preamplifiers offer a good compromise between noise performance and power consumption. Using an external load capacitance of 150 pF at the input, and the shaping amplifier described below, the noise is typically 0.6 fC fwhm (1600 electrons rms), at

27 mW/channel. The gain is ~ 0.7 mV/fC and the output is able to drive a capacitive load of several hundred pF without risk of oscillations, but it cannot drive a terminated line.

3.4 The shaping amplifier and track-and-hold circuits.

The optimum shaping time constant τ depends on the preamplifier input FET and on the detector capacitance and leakage current. In our case the noise as a function of τ has a flat minimum typically between $0.5 \mu\text{s}$ and $1 \mu\text{s}$. We use a hybrid circuit, with a double differentiating and double integrating shaping stage ($\tau_{\text{diff}} = \tau_{\text{int}} = 0.73 \mu\text{s}$) followed by a track-and-hold circuit. In the track-mode the width of the shaped signal is $2 \mu\text{s}$ at half amplitude and $4 \mu\text{s}$ at the base. This is compatible with the $4 \mu\text{s}$ beam structure of the $p\bar{p}$ -collider. The output amplitude is 25 mV/fC.

After each beam crossing the signal amplitude from each pad is held until the trigger decision is made. After a valid trigger the voltage levels at the track-and-hold amplifier outputs are digitized sequentially as discussed below; otherwise the circuits are switched back to the track-mode. The switching speed of the track-and-hold circuit is well adapted to the signal shape and the Collider beam structure. The output sag during the 1 ms long hold-phase needed for the multiplexed readout is negligible.

3.5 Multiplex readout

The signals of the 63 pads of each module are digitized successively by a single fast encoding and readout ADC [8].

Only three 16-channel ADC-modules and 48 signal lines are needed for the whole detector. The scanning of the 63 signals per module is performed using four analog CMOS multiplexers (see fig. 7).

The results of the 48 conversions at each step of the multiplex sequence are transferred via the ECL-bus to the raw data memory. The multiplex addresses and the ADC gate and clear signals are generated by a NIM-module, the MUX-controller. About 1 ms after a trigger signal the digitisation of the 3024 signals is completed, with a resolution of 11 bits.

4. OPERATION AND PERFORMANCE.

The first complete module, with 9 counters, was installed in the UA2 detector and operated for 110 days of $\bar{p}p$ Collider running between September and December 1985. A further two modules, each equipped with 8 detectors, were installed during the run and continuously operated for 65 days. Throughout this period, the counters were biased at a constant voltage. During $\bar{p}p$ runs a beam crossing took place every $8 \mu\text{s}$ and the UA2 trigger rate was $\sim 10 \text{ Hz}$.

4.1 Monitoring.

During the 65 - day period when all three modules were installed, a total of 166 pads (including some pads not satisfying the criteria of section 2) were connected. The pads were operated at an ambient temperature of $\sim 35^\circ\text{C}$ (the final array will be operated at $\leq 20^\circ\text{C}$). Throughout the run, the temperature and the leakage current of each board was monitored.

The pedestal position and width of each pad was measured every 5 hours, and a stability monitor of these quantities proved a reliable indicator of the quality of the array. The typical pedestal width, σ_{ped} , was $\sim 8\%$ of the response of a minimum ionising particle (mip). At the end of the run, 153 pads operated satisfactorily ($\sigma_{\text{ped}} < 0.16 \text{ mip}$) and in every case, the value of σ_{ped} described the pad performance accurately. The rms of successive σ_{ped} measurements was on average 0.02 mip (spread 0.025 mip) for the 166 connected pads.

4.2 Calibration

The final calibration of the full array will be performed in a test beam. Since this was not possible prior to $\bar{p}p$ operation, the present array was calibrated using a set of 10^5 typical $\bar{p}p$ interactions. Tracks are reconstructed in the UA2 vertex detector, and the impact position on the silicon array is evaluated. The pulse-height, PH1, of the pad indicated by track reconstruction is recorded. Because of limited track precision the pulse height of the neighbour pad nearest to the impact point is also found (PH2). In fig. 8 the value of PH2 is plotted against PH1, after correcting for the dependence of pulse height on the crossing angle of the track. This shows

- i. the expected Landau distribution from minimum ionising particles, well separated from the pedestal in PH1,
- ii. a similar distribution in PH2,
- iii. a small pedestal due to incorrectly reconstructed tracks,
- iv. a number of hits in which the charge is shared between the neighbouring pads (these hits are found to lie near the pad edges).

The calibration constants for each pad were determined by fitting such PH1 distributions pad by pad, requiring that no hit ($> 3 \sigma_{\text{ped}}$) occurs in the neighbouring pad (PH2). The mean response of the channels was 2.86 ADC counts/keV of energy deposited in the silicon, with an rms variation between channels of 0.26 ADC counts/keV. These results are insensitive to the contamination of the signal by hits from two minimum ionising particles (eg. from photon conversions), and are consistent with the expected values, taking into account the sensitive thickness of each counter and the gain of the corresponding electronics channel. The gains were monitored during the run using a pulse generator. Fig. 9 shows the calibrated pulse height distribution. The left width at half maximum of the signal is 16% of a mip. An excess of events at large pulse-height, due to contamination from two

or more particles traversing the pad, makes an accurate determination of the true rejection power of the array against photon conversions impossible from these data.

4.3 Efficiency and occupancy.

Using the 153 satisfactory pads noted in section 4.1, the inefficiency of the silicon array to charged particles traversing it was estimated from a sample of well reconstructed tracks. The measured inefficiency was $2 \pm 2\%$, consistent with the number of false tracks in the sample.

The pattern of tracks and silicon pulse heights ($> 3 \sigma_{\text{ped}}$) is shown in fig. 10 for an event of the type $\bar{p}p \rightarrow W^\pm + \text{anything}$; $W \rightarrow e\nu$, in which the electron traverses the silicon. Two pads, each with an associated charged track, have a pulse height exceeding $3 \sigma_{\text{ped}}$. The average occupancy for typical $\bar{p}p$ interactions is 1.6%, consistent with the signal - to - noise ratio of approximately 13 : 1.

5. CONCLUSIONS.

We have described the status of construction of a 1 m^2 silicon array, to be used for particle ionisation and position measurements in the UA2 apparatus at the CERN $\bar{p}p$ Collider.

The feasibility of constructing and operating such an array has been demonstrated by installing a fraction of the array at the Collider in a 110-day period from September to December, 1985. Despite non-optimum conditions (in particular a high ambient temperature), the array operated with excellent stability.

On the basis of existing data, we have shown that the array can be monitored reliably from checks of the pedestal width for each channel.

The array provides space points for track reconstruction with an efficiency exceeding 98%, and a high signal - to - noise ratio (13 : 1). It will enable the discrimination of photon conversions and Dalitz decays from single electrons.

ACKNOWLEDGEMENTS

We wish to thank the staffs of the Bern and CERN institutes participating in UA2 for their contributions to the construction of this detector.

The contributions of J.R. Hansen and L. Mapelli during the 1985 $\bar{p}p$ run are warmly acknowledged.

We wish to thank H. Plathow-Besch for her significant contributions during the initial phase of this project.

Financial support from the Schweizerischer Nationalfonds zur Förderung der Wissenschaftlichen Forschung to the Bern group, and from the CERN management, is gratefully acknowledged.

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FIGURE CAPTIONS

1. Layout of the silicon array.
2. Photograph of a silicon counter, showing seven independent segments (pads) and a guard ring surround is the detector.
3. a) Reverse current as a function of bias voltage.
b) Capacitance as a function of bias voltage. The curves are shown with the numerical offset listed on the figure.
4. Distribution of full depletion voltage for 143 silicon counters.
5. Distribution of reverse current at full depletion (measured at 19° C) for 1001 pads of 143 counters.
6. Photograph of a fully assembled motherboard, and its associated electronic box.
7. Block diagram of the electronic readout.
8. The pulse height distribution PH1 (ADC units) of the pad corresponding to the reconstructed track impact, versus the pulse height PH2 of its nearest neighbour.
9. The calibrated pulse height distribution, in ADC units.
10. Silicon hits associated with an event $\bar{p}p \rightarrow W^{\pm} + \text{anything}; W \rightarrow e\nu$, in which the electron traverses the silicon array.

Fig. 1

Fig. 2

Fig. 3a

Fig. 3b

Fig. 4

Fig. 5

Fig. 6

Fig. 7

Fig. 8

Fig. 9

Fig. 10