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A via last TSV process applied to ATLAS pixel detector modules: proof of principle demonstration

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ABSTRACT: Via last Through Silicon Vias (TSVs) can be exploited to build low material modules for the upgrades of the ATLAS pixel detector at the High Luminosity LHC. To prove this concept a via last TSV process is demonstrated on ATLAS pixel readout wafers. Demonstrator modules featuring 90 μm thin readout chips with TSVs are operated using the connection from the back side of the chip. This paper illustrates the via formation process and the results from the characterization of modules with TSVs.

KEYWORDS: Detector design and construction technologies and materials; Hybrid detectors; Particle tracking detectors (Solid-state detectors)

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1 Introduction

The processing of Through Silicon Via (TSV) is of fundamental importance for the success of 3D integration, where TSVs provide a high density vertical interconnection for the stacking of different electronic tiers. In the field of High Energy Physics (HEP) experiments, TSVs can be used in the design of innovative module concepts for hybrid pixel detectors. The work presented in this paper demonstrates a via last TSV¹ process on ATLAS pixel Front-End (FE) electronics, as a viable technology to develop a module design with minimal material for the upgrades of the detector at the High Luminosity LHC (HL-LHC) [1]. Figure 1 shows a sketch of a possible module concept with via last TSVs, together with a module of the Insertable B-Layer (IBL)² for comparison. Vias are etched under the chip peripheral bond pads to bring the electrical connection to the chip back side. Here a Re-Distribution Layer (RDL) can be used to route signals and power to/from the detector services. Passive components can be bonded on the signal lines on the FE back side. With respect to today's hybrid pixel modules ([2, 3]), this module concept allows reducing the area of the chip periphery, and does not require interconnect flex nor connectors to interface the module to the services. The detector services can run directly on the FE back side, and be wire bonded here to the pads, reducing as well the module envelop. This results in a low mass, compact module design with easy connection to the outside world, with minimal modification to the traditional FE layout and using standard CMOS technology. This paper illustrates the selected via last TSV process, and the steps for via formation on ATLAS FE-I3 readout wafers [4]. Demonstrator modules with 90 μm thin FE-I3 readout chips and tapered profile TSVs have been built and successfully operated using the electrical connection on the chip back side. The work is carried out in collaboration by the University of Bonn and the Fraunhofer Institute for Reliability and Microintegration (IZM, Berlin).

¹Via last TSVs are formed on the fully processed IC wafer, in opposition to via first TSVs where the vias are formed during CMOS processing.

²The IBL is the first upgrade of the ATLAS pixel detector. It adds a fourth pixel layer to the present detector at a radius of 3.7cm, together with a new smaller beam pipe.

Figure 1. Sketch of a module concept with TSVs (left) and of an IBL module (right), showing the advantages of a module design with TSV. The size of the periphery can be reduced in the TSV module as the front side bond pads are not used for wire bonding. The connection to the detector services can be made less bulky, using only RDL and wire bonds on the FE backside, instead of interconnect flex circuits bending over the stave edge. The overall reduced module envelop is beneficial given the tight space constraints imposed by the detector layout.

2 Via last TSVs on ATLAS readout wafers

Two via last TSV processes developed by IZM have been investigated for prototyping with the ATLAS pixel FE electronics, namely straight side wall and tapered side wall TSVs. The first makes use of a standard Bosch process [5], in which etching and passivation steps are alternated. Tapered side wall vias are instead etched in one step and passivation is deposited at the end of the etching process. Both processes have been demonstrated on monitor wafers and typical via profiles are shown in figure 2. In the case of via last TSVs, the via diameter can be relaxed up to the bond pad size, typically 100–150 μm , provided process parameters allow for these via features. The processing time and the available tools determine in fact the achievable quality of the via shape, as well as the homogeneity in the deposition of the isolation layer, on the via side wall and bottom, and of the plating base, across the entire wafer. This in turn sets limits on the aspect ratio that the process can be tuned for. In the straight profile TSV process studied here, the achievable aspect ratio is from 2:1 to 5:1, where the standard parameters are 20 μm via diameter and 100 μm depth. In the tapered via process, side wall angles of about 60–70° can be achieved. With a maximum via top diameter set in this case by the bond pad pitch (approx. 150 μm), the via depth is in the order of 80–150 μm , with via bottom diameters of 30–40 μm . Current developments at IZM aim at 300 μm depth for a 150–200 μm top diameter.

The tapered side wall process has been selected to prototype demonstrator TSV modules with the ATLAS FE-I3 electronics, as it allows for a simpler deposition process of the isolation layer with respect to straight side wall TSVs, using thin film polymers. A batch of two FE-I3 wafers has been processed. The via formation process on these wafers requires both a front side and a back side processing. In this FE design, only the last metal layer is present in the bond pad. Front side processing is thus needed to connect the aluminum bond pad on the front side to the via. A so-called plug is used for the connection. The plug formation is done first, before wafer thinning. The aluminum pad is opened by a wet etching process. The BEOL³ SiO₂ is then etched up to

³Back End Of Line (BEOL) is a step in the IC fabrication process where the individual devices, such as transis-

Figure 2. Example of straight (left) and tapered (right) side wall TSVs on a monitor wafer. The straight profile TSV has a depth of approximately $60\text{ }\mu\text{m}$ and an opening of $30\text{ }\mu\text{m}$. For the tapered TSV, bottom and top via diameters are respectively of 41 and $95\text{ }\mu\text{m}$, the side wall angle is 70° , and the wafer thickness is $77\text{ }\mu\text{m}$.

Figure 3. Front side processing on the ATLAS FE-I3 wafers. From left to right: Al pad opening, BEOL SiO_2 etch, plug formation.

the Si interface, and the plug is formed by electroplating of copper. Figure 3 shows the front side processing steps on the processed ATLAS FE-I3 wafers.

After completion of the plug, the back side processing starts, i.e. the actual process of via formation [6, 7], from wafer thinning to RDL, including:

- Carrier bonding on the front side for handling and mechanical support of the thinned wafer. For this a perforated glass carrier with polymer bond has been used;
- Si back side thinning. The target thickness for the processed wafers is $90\text{ }\mu\text{m}$;
- Si etch profile for tapered side wall vias using Deep Reactive Ion Etching (DRIE);
- Via side wall passivation using a PECVD (Plasma Enhanced Chemical Vapor Deposition) oxide layer and a polymer layer;
- Opening of the passivation on the via bottom;
- Barrier seed layer deposition (sputter deposition of TiW/Cu plating base);
- Via coverage by Cu electroplating;

tors, resistors and capacitors, are connected using metal interconnect layers. It follows the Front End Of Line (FEOL) processing where the devices are formed on the Si wafer.

Figure 4. Tapered profile TSV and plug on the FE-I3 wafers.

Figure 5. RDL and wire bond pads on the FE-I3 back side.

- Patterning of back side RDL and bond pad preparation. The metal used is gold in order to have wire bondable pads;
- Bonding of carrier on the wafer back side for further processing;
- Solvent based debonding of the carrier on the front side.

Figure 4 shows the tapered via profile on the FE-I3 wafers, together with the plug on the front side. Top and bottom via diameters are approximately 45 and 110 μm .

The RDL and bond pad structure on the FE back side are shown in figure 5. For this first demonstrator TSV modules, a simple RDL pattern is chosen which reproduces the front side bond pads. The bond pads on the back side are located on top of the pixel matrix to be supported by the sensor during wire bonding of the modules on a PCB for testing.

Figure 6. Noise map (left) and noise distribution (right) of a TSV module. Connected pixels, in the center of the pixel matrix, have higher noise as the connection to the sensor increases the input capacitance seen by the preamplifier.

The wafer is then processed for bump bonding to a sensor tile for module assembly. For this TSV proof of principle demonstration, where the main interest is the validation of the TSV process only, a standard flip chip process is used consisting of bump deposition, back side carrier debonding and wafer dicing. The FEs are then flip-chipped on the sensor tiles, and the assembly is finally mated in a reflow process. No handle wafer was used during reflow as it is normally the case for thinned ATLAS chips. It is therefore expected that the thin FE bends up at the corners due to the high temperature used in the reflow process (in this case up to 260°C). As a consequence only an area in the center of the pixel matrix is connected to the sensor. IZM developed a flip chip process for large, thin IC. It uses a glass carrier bonded to the wafer back side with a 10 μm layer of laser releasable polymer material [8]. The glass carrier is released via laser exposure only after reflow. Flip chip of thin ICs with this process is used to build modules for the IBL project using the FE-I4 readout chip [1, 3]. The combination of the two processes, via formation and flip chip of thin ICs, is possible but it requires a further demonstration step, as the topography on the TSV chip back side (i.e. the RDL) sets constraints on the polymeric glue thickness and the uniformity of the deposition.

3 Results of electrical tests on demonstrator TSV modules

The TSV modules are wire bonded onto a dedicated PCB, using the bond pads on the FE back side, i.e. the TSV connection is used to operate the module. Figure 6 shows a noise map of the FE. Two areas can be clearly distinguished, with different noise values, indicating connected pixels at the center of the module, and unconnected pixels along the perimeter of the FE, as expected. Noise figures for both connected and unconnected pixels are approximately 180e⁻ and 130e⁻, respectively, and compare well with the noise figures from FE-I3 bare chips and modules operated with the standard front side connection [9]. The module can be operated with threshold values down to 2000e⁻, in agreement with what observed on ATLAS pixel FE-I3 modules [9].

To assess full module operation, the spectrum of a radioactive source (60keV gamma rays) is recorded. The spectrum is shown in figure 7 demonstrating that the TSV processing was successful throughout, such that the operation of the module suffers no loss in performance.

Figure 7. Spectrum of an Am-231 source recorded with a demonstrator module with TSVs (no clustering applied).

4 Conclusions

Via last TSVs are proposed as a technology to build modules with minimal material for the upgrades of the ATLAS pixel detector. A via last TSV process has been developed by the University of Bonn and the Fraunhofer Institute for Reliability and Microintegration, and has been successfully prototyped with ATLAS readout electronics and pixel modules. This constitutes a first proof-of-principle of this technology for future pixel module concepts. The modules operated using the TSV contacts show no loss in performance compared to standard ATLAS pixel modules operated using the connection on the front side of the readout chip. The process will also be demonstrated on the next generation ATLAS pixel readout chip, the FE-I4 [3], developed for the upgrades of the detector at the HL-LHC. This FE chip has already been designed to accommodate TSV connection (i.e. the first and last metal layers in the pad are connected), and thus does not need front side processing (for the plug). The combination of the TSV process and the flip chip of thin ICs using the laser releasable polymer bond technology will also be demonstrated on TSV modules with 90 μm thin FE-I4.

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