A Highly Parallel FPGA Implementation of a 2D-Clustering Algorithm for the ATLAS Fast Tracker (FTK) Processor

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**Summary**

- Several prototype of FTK IM have been produced and tested.
- The boards work well with fiber input at 2.0 Gbps and 200 MHz DDR output.
- Data communication shows no error after 10¹⁰ bits are transfer, which meets the requirement from the ATLAS experiment.

**1. FTK IM**

- Single and multi engine clustering algorithm was tested on firmware simulation with expected data.
- Single engine 2D Clustering algorithm work perfectly with real S-LINK inputs as tested at CERN.
- The implementation of 16 parallel engines was prepared. It occupies 40% of a FPGA resource. A 4 parallel engines implementation is sufficient for Pixel inputs. Studies for IBL inputs are in progress.
- The parallelized 2D clustering implementation has a enough processing power for 80 pile-up that correspond to the maximum LHC luminosity planned until 2022.

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**FTK Input mezzanine board (FTK IM)**

- **FTK IM is the most upstream board of FTK system.**
- **The board was developed to receive all ATLAS Inner Detector data read out at event rate of 100 kHz and to perform clustering.**
- **Total 128 FTK IMs receive total ~800 S-LINKs (maximum 2.0 Gbps, 32 bits word 40 MHz)**
- **FPGAs perform clustering of Inner Detector hit information**
- **The clustered 32 bits data word are sent to FMC connector at 50 MHz over a 200 MHz DDR 8 bit bus.**

**FTK**

- **FTK is an approved ATLAS trigger upgrade project. It provide all track information (pT > 1 GeV) for any event accepted by Level 1 trigger.**
- **Provided track information is used by High Level Trigger (HLT) for efficient triggering.**
- Highly parallelized hardware system

**Clustering Algorithm**

- Clustering signifies identification of the group of contiguous hits from inner track detector.
- The clustering implementation is designed in three separate processing modules of the hit decoder module, the grid clustering module, the centroid calculation module, and grid-clustering engine module. Multiple clustering engines can work in parallel.
  1. **Hit Decoder**
     Hit decoder decodes ATLAS format to a format useful for the clustering, and re-aligns incoming hits to pixel column sequence.
  2. **Grid Clustering**
     Grid clustering uses a “moving window” technique to minimize computational time per cluster identification as well as needed FPGA resources.
  3. **Centroid Calculation**
     Centroid calculation calculate the centroid including a correction based on Time-over-threshold information, which is correlated to the charge collected by each pixel.

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**Test Setup at CERN**

<table>
<thead>
<tr>
<th>Parallel engine</th>
<th>1</th>
<th>4</th>
<th>16</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPGA resource occupancy</td>
<td>3%</td>
<td>11%</td>
<td>40%</td>
</tr>
</tbody>
</table>

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**FTK Input mezzanine board (FTK IM)**

- **Fast and Efficient Clustering!**
- **344x128 pixels**
- 768 strips
- FPGA (Spartan-6 LX150T)
- Insertable B-Layer: 14 Stage, 12 M channel, 56 Read out S-LINKs
- Each FPGA cluster data from one SCT and one pixel link.
- **Total 128 FTK IMs receive total ~400 S-LINKs (maximum 2.0 Gbps, 32 bits word 40 MHz)**
- **FPGAs perform clustering of Inner Detector hit information**
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**FTK**

- **Pixel Module**
  - Each FPGA cluster data from a 200 MHz DDR 8 bit bus.
- **ROD Hit Decoder**
  - **The first processing step of the FTK is the clustering of strip and pixel data that reduces due amount of data to be processed by downstream algorithm and provides an accurate estimate of the cluster centroid.**

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**FTK Input mezzanine board (FTK IM)**

- **Very fast tracking!**
- **Highly parallelized hardware system**
- **2.1 m**
- **Total 128 FTK IMs receive total ~80 M channel**
- **FTK system.**

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**Summary**

- **The LHC after the 2013-2014 shutdown periods is expected to deliver an increased instantaneous luminosity, which will make more difficult to have efficient online selection of rare events due to increasing of pile-up (60 or more proton-proton collisions overlapping in the same bunch crossing).**
- **Real time tracking information by Fast Tracker (FTK) system make possible new trigger selections, which are robust against pile-up.**

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Hard to select important physics event with many overlapping proton-proton collision (pile-up).

It points to the critical need for highly parallelized hardware system and 2D clustering algorithm implementation!

Real-Time processing is necessary for online event selection!

How to cluster about 500 Gbps 2D hits using FPGAs
A 4 parallel engines implementation is sufficient for Pixel inputs for pile-up 80 that correspond to the maximum LHC luminosity planned until 2022.