A Highly Parallel FPGA Implementation of a 2D-Clustering Algorithm for the ATLAS Fast Tracker (FTK) Processor

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Idea of the 2D-Clustering implementation

$Z \rightarrow \mu+\mu$ -@ pile-up ~60

- The LHC after the 2013-2014 shutdown periods is expected to deliver an **increased instantaneous luminosity**, which will make **more difficult** to have efficient **online selection** of rare events due to increasing of **pile-up** (60 or more proton-proton collisions overlapping in the same bunch crossing).
- Real time tracking** information by **Fast Tracker (FTK)** system make possible new trigger selections, which are **robust against pile-up**.

The first processing step of the FTK is the clustering of strip and pixel data that reduces the amount of data to be processed by downstream algorithm and provides an accurate estimate of the cluster centroid.

Fast Tracker (FTK)

- FTK is an approved ATLAS trigger upgrade project. It **provide all track information** ($P_T > 1$ GeV) for any event accepted by Level 1 trigger.
- Provided track information is used by **High Level Trigger (HLT)** for **efficient triggering**.

Highly parallelized hardware system

Very fast tracking!

FTK Input mezzanine board (FTK IM)

Pixel :
Total 1744 modules
~80 M channel
194 Read out S-LINKs

344x128 pixels

Insertable B-Layer :
14 Stave
12 M channel
56 Read out S-LINKs

- FTK IM is the **most upstream board** of FTK system.

- The board was developed to **receive all ATLAS Inner Detector data** read out at event rate of 100 kHz and to perform **clustering**.

Strip Module

768 strips

FPGA (Spartan-6 LX 150T)

Fast and Efficient Clustering!

SCT :
Total 4088 modules
~7.5 M channel
128 Read out S-LINKs

Huge channel Heavy input

S-LINK Receiver

FMC Connector

- Total 128 FTK IMs receive total ~400 S-LINKs (maximum 2.0 Gbps, 32 bits word 40 MHz)
- FPGAs **perform clustering** of Inner Detector hit information
- The clustered **32 bits data word** are sent to FMC connector **at 50 MHz** over a 200 MHz DDR 8 bit bus.

Clustering Algorithm

- Clustering signifies identification of the group of contiguous hits from inner track detector.

- The clustering implementation is designed in three separate processing modules of the **hit decoder** module, the **grid clustering** module, the **centroid calculation** module, and **grid-clustering engine** module. Multiple clustering engines can **work in parallel**.

1. Hit Decoder

Hit decoder decodes ATLAS format to a **format** useful for the **clustering**, and **re-aligns** incoming hits to pixel **column sequence**.

2. Grid Clustering

Grid clustering uses a **“moving window”** technique to minimize computational time per cluster identification as well as needed **FPGA resources**.

3. Centroid Calculation

Centroid calculation calculate the centroid including a correction based on **Time-over-threshold** information, which is correlated to the charge collected by each pixel.

Summary

FTK IM

- Several **prototype of FTK IM** have been produced and tested.
- The boards work well with fiber **input at 2.0 Gbps** per line and **200 MHz DDR output**.
- Data communication shows **no error after 10¹⁶** bits are transfer, which meets the requirement from the ATLAS experiment.

Pixel Clustering Algorithm

- Single and multi **engine Clustering algorithm was tested** on firmware simulation with expected data.
- Single engine** 2D Clustering **algorithm work perfectly** with **real S-LINK inputs as tested at CERN**.
- The implementation of **16 parallel engines** was prepared. It occupies **40 % of a FPGA resource**. A 4 parallel engines implementation is sufficient for Pixel inputs. Studies for IBL inputs are in progress.
- The parallelized 2D clustering implementation has a **enough processing power** for 80 pile-up that correspond to the maximum **LHC luminosity planned until 2022**.

Test Setup at CERN

Parallel engine	1	4	16
FPGA resource occupancy	3%	11%	40%

is necessary
on!

FPGA
(Spartan-6 LX 1501)

4 inputs

Huge channel
Heavy input

S-Link Receiver

FMC Connector

	3	9	7						
	1					13	15		
	4	8	6	11					
							12		
0	1	2	3	4	5	6	7	8	9

Poster

Introduction and Motivation

Hardware system

How to cluster

Test Results and summary

Parallel engine	1	4	16
FPGA resource occupancy	3%	11%	40%

A 4 parallel engines implementation is sufficient for Pixel inputs for pile-up 80 that correspond to the maximum LHC luminosity planned until 2022.