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The eCDR, a Radiation-Hard 40/80/160/320 Mbit/s CDR with internal VCO frequency calibration and 195 ps programmable phase resolution in 130 nm CMOS

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ABSTRACT: A clock and data recovery IP, the eCDR, is presented which is intended to be implemented on the detector front-end ASICs that need to communicate with the GBTX by means of e-links. The programmable CDR accepts data at 40, 80, 160 or 320 Mbit/s and generates retimed data as well as 40, 80, 160 and 320 MHz clocks that are aligned to the retimed data. Moreover, all the outputs have a programmable phase with a resolution of 195 ps. An internal calibration mechanism enables the eCDR to lock on incoming data even without the availability of any form of reference clock. The radiation-hard design, integrated in a 130 nm CMOS technology, operates at a supply voltage between 1.2 V and 1.5 V. The power consumption is between 28.5 mW and 34.5 mW, depending on the settings. The eCDR can achieve a very low RMS jitter below 10 ps.

KEYWORDS: Analogue electronic circuits; Data acquisition circuits; Radiation-hard electronics

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1 Introduction

The eCDR (CDR for Clock and Data Recovery) has been developed in the framework of the GBT project, which is currently under development as part of the Large Hadron Collider (LHC) upgrade program. The GBT project aims at the realization of a radiation-hard chipset to be used as an on-detector transceiver for the LHC experiments. A bi-directional optical link operating at 4.8 Gbit/s connects this transceiver, the GBTX, with the counting room. On the other side, up to 56 front-end modules can be connected to the GBTX by means of electrical links (e-links) [1].

A full-blown e-link is composed of 3 differential lines, 1 for the uplink, 1 for the downlink and 1 for the clock signal that is sent to the front-end module by the GBTX. In that case, the data recovery in the front-end module is easy to do since the received clock signal can be used directly to retime the data. However, if cabling is difficult or critical, one might prefer to remove the clock differential line. In that case, to recover the data in the front-end module, a proper clock signal needs to be generated first, after which the received data can be retimed with that clock. This is exactly the purpose of the eCDR.

Since the e-links have a programmable data rate of 80, 160 or 320 Mbit/s, the eCDR has been conceived as a highly flexible clock and data recovery system. It accepts input data at 40, 80, 160 or 320 Mbit/s and outputs the retimed data along with a 40, 80, 160 and 320 MHz output clock, regardless of the data rate. The phase of the output data and the 4 output clocks, which are always in-phase, can be programmed with a resolution of 195 ps, so they can easily be aligned with any other clock domain in the front-end module if required.

The architecture of the eCDR is presented in section 2, some of the building blocks are discussed in section 3 and the measurement results are shown in section 5. A conclusion is drawn in section 6.
2 System overview

The block diagram of the eCDR is shown in figure 1. The input data is applied to a set of detectors: a Phase Detector (PD) and a Frequency Detector (FD). These detectors each control their own charge pump that charge or discharge the first-order loop filter. The Voltage Controlled Oscillator (VCO), which always oscillates at 320MHz regardless of the data rate, is an 8-stage differential ring oscillator and generates 16 phases of the 320MHz clock. The required programmability of the data rate is enabled by means of a programmable feedback divider with a ratio of 1, 2, 4 or 8. It generates both an in-phase and a quadrature version of the divided clock.

The data is retimed within the PD as can be seen in figure 1. It is in-phase with the feedback in-phase clock which is fed to the PD. In a typical CDR system, this retimed data and feedback clock would be the output signals. In the presented eCDR however, extra functionality is provided by means of the phase shifter. The phase shifter is intended to shift the phase of the extracted clocks and the retimed data so as to be able to align them with whichever clock in the system. In order to do that, it utilizes the 16 phases of the VCO to enable a phase shifting with a resolution of 195ps, namely 1/16th of the 320MHz clock.

The Alexander PD, and basically any PD that can work with data, suffers from the fact that it cannot correct any frequency difference between the input data and the VCO. Consequently, the acquisition range of the eCDR with only the PD would be extremely limited. Therefore, a rotational FD has been added in the eCDR which is based on ref. [3]. As such, the acquisition range is increased significantly up to about ±25% of the data rate.

The eCDR incorporates 2 possibilities to bring the VCO frequency within the acquisition range of the CDR loop. Both are highlighted in gray in figure 1. The first possibility is to start the loop in the PLL-mode before applying any input data. In that case, the PD and FD are disabled and the PFD, which reuses the PD charge pump, is enabled. As the PFD has an acquisition range that is basically unlimited, the VCO frequency will be brought to the applied clock frequency in
3 Building blocks

3.1 Detectors

3.1.1 PD

A block diagram of the Alexander PD inside the eCDR can be seen in figure 2. This bang-bang PD makes a decision (up/down) for every transition in the input data. If there is no data transition, both the up and the down signal remain low. Assuming that there is only a phase offset between the clock and the input data, the up and down signals can never be high at the same time.

As shown in figure 2, 3 samples of the input data are used, 2 rising edge samples, S₁ and S₃ and 1 falling edge sample, S₂. If S₁ and S₂ differ, a data edge has appeared in between them and the falling clock edge came too late. An up signal is generated to increase the VCO frequency. On the contrary, if S₂ and S₃ are different, the falling edge came too early and a down signal is generated. In any of both cases, this PD tries to push the falling edge of the clock towards the data edges so that the data can reliably be sampled by the rising clock edge. As a result, S₁ and S₃ are reliable and retimed versions of the input data and either of them can be used as output data.

Figure 2. Block diagram and working principle of the Alexander PD in the eCDR.

Figure 3. Block diagram of the rotational FD in the eCDR.
3.1.2 FD

The FD, a block diagram of which is shown in figure 3, has a rotational architecture [3]. The 4th (Q4) and 1st (Q1) quadrant of the VCO clock are sampled at every rising and falling data edge. An up pulse is generated if and only if a data edge samples the clock in Q1 while the next data edge samples the clock in Q4. Logically, this can only happen if there is a frequency offset between the VCO clock and the input data. In this case, the VCO clock is too slow because the VCO phasor did not complete the full 360° between 2 consecutive data edges. Consequently, an up pulse is necessary to make the VCO oscillate at a higher frequency. On the contrary, a down pulse is generated if and only if a data edge samples the clock in Q4 while the next data edge samples the clock in Q1. The VCO frequency is thus too high and needs to be decreased.

In order for the FD in figure 3 to generate pulses, the frequency error may not be too large. For example, if 2 consecutive data edges sample Q1 and Q3 respectively, instead of Q1 and Q4, no up pulse is generated, although the VCO frequency is clearly too low. It means that this frequency offset is too large for this type of FD to detect. The same is true for a too high VCO frequency that does not generate any down pulses. It can be reasoned that the VCO frequency range for which this rotational FD generates a useful output is approximately ±25% of the data rate.

The number of pulses that is generated by the FD depends on the frequency offset. The larger the offset, the more frequently the data phasor crosses the Q4-Q1 border leading to a lot of up or down pulses. On the contrary, for a zero frequency offset, no pulses are generated at all. The PD, which is only sensitive to phase errors, then takes over to bring the data phasor towards the Q2-Q3 border so that the input data can be sampled by the rising edge of the clock. The loop that is formed by the FD thus opens automatically once the PD loop has found lock.

3.2 Wien bridge calibration

The Wien bridge calibration circuit is shown schematically in figure 4. The working principle is to equalize the voltages of the Wien bridge, one half of which is composed of resistors $R_1$ and $R_2$, the other half being composed of resistor $R_{trim}$ and switched capacitor $C_{sw}$. For a switching frequency $f_{sw}$, the equivalent resistance of the switched capacitor can be calculated as follows:

$$R_{eq} = \frac{1}{f_{sw}C_{sw}}. \quad (3.1)$$

In steady-state, the closed loop, consisting of the Wien bridge, integrator, VCO and frequency divider, establishes a control voltage to the VCO which is such that it oscillates at the frequency that
keeps the Wien bridge in equilibrium, i.e. the 2 voltages being equal. This equilibrium frequency can be calculated as follows:

\[ f_{\text{sw,eq}} = \frac{R_2}{R_1 R_{\text{trim}} C_{\text{sw}}} \]  

(3.2)

Since the VCO has to be calibrated to 320MHz and due to the fixed divider ratio of 8 in the calibration loop, the wanted \( f_{\text{sw,eq}} \) is 40MHz. In the eCDR, \( R_1 \) equals \( R_2 \) resulting in an equilibrium voltage that is half the supply voltage. Since \( R_{\text{trim}} \) has a mid-scale resistance of 18kΩ, \( C_{\text{sw}} \) needs to be 1.4pF for \( f_{\text{sw,eq}} \) to equal 40MHz. In order to correct for process variations and integrator offset, \( R_{\text{trim}} \) can be programmed between 12.5kΩ and 25kΩ with a resolution of 190Ω.

After a reset, \( C_{\text{lpf}} \), the eCDR loop filter capacitor, is discharged and, as a result, the VCO does not oscillate. The Wien bridge is not in equilibrium as its right node is pulled to ground by \( R_{\text{trim}} \). As a result, the integrator charges \( C_{\text{lpf}} \) and the VCO control voltage rises. When it reaches a certain value, the VCO starts oscillating and the right Wien bridge node voltage rises thanks to the decreasing equivalent resistance of the switched capacitor. This goes on until the Wien bridge is in equilibrium and the integrator remains stable. In the case where the right node is higher than the left node in the Wien bridge, \( C_{\text{lpf}} \) is discharged, the VCO frequency decreases and both bridge nodes are steered to equilibrium again.

As can be seen in figure 4, a capacitor \( C_f \) has been added to create a pole at the right Wien bridge node. Such a pole is necessary in order for that node to partly retain its voltage when switching \( C_{\text{sw}} \). Otherwise, \( R_{\text{trim}} \) would always bring that node back to ground and the calibration circuit would never settle. The introduced pole should therefore be considerably smaller than the intended \( f_{\text{sw,eq}} \). However, stability issues might show up by adding this pole in the feedback loop. Note that the integrator already has a pole at DC so the extra pole should be at a frequency that is high enough. This can be achieved by decreasing the integrator gain or by decreasing \( C_f \).

As mentioned before, process variations and integrator offset can be tuned out by means of \( R_{\text{trim}} \) as they are known before actually using the eCDR. More important are the variations that can appear during operation, namely temperature and supply voltage fluctuations. Due to the architecture of the Wien bridge, namely that only the voltage difference between the left and right nodes is considered, the supply voltage does not have an effect on \( f_{\text{sw,eq}} \) as long as the integrator has sufficient gain. The sizing of the switches in figure 4 has been shown to be critical for the temperature stability of \( f_{\text{sw,eq}} \) [4]. The switches should not be too small as the ON resistance can become too high to fully charge/discharge \( C_{\text{sw}} \) in half of the period of \( f_{\text{sw,eq}} \). However, thanks to the 1/8 divider, the full 12.5ns are available for this. As a result, the ON resistance can be quite high without affecting the performance of the circuit. The switches should neither be too large since their leakage currents, which exponentially depend on temperature, alter \( f_{\text{sw,eq}} \). Therefore, the OFF resistance should be several orders of magnitude higher than \( R_{\text{eq}} \).

4 Parameter selection

The eCDR is intended to be operated from a wide range of supply voltages between 1.2V and 1.5V. On top of that, it should work over a temperature ranging from −30°C to 100°C and obviously all possible process corners. One of the major consequences of these widely varying conditions is that
the gain of the VCO will shift dramatically, according to simulations between $182\text{MHz V}^{-1}$ and $1200\text{MHz V}^{-1}$. As can be expected, such a large spread on the VCO gain has its effects on the loop dynamics. On top of that, the loop dynamics depend strongly on the data rate (feedback divider ratio) and its transition density. The more transitions there are, the more decisions the PD makes and the more frequently the VCO is steered towards the correct phase. On the contrary, if there are no data transitions, the PD makes no decisions at all and the loop behaves as being open. The VCO phase will drift significantly in that case. When designing the eCDR, a transition density of 50% has been assumed, which is a typical value for random data.

In order to make sure that the eCDR can lock and behave properly in all these situations, the loop filter resistance can be programmed between 0.5 kΩ and 8 kΩ. On top of that, the 2 charge pumps have an independently programmable output current between 0.8 µA and 12 µA for the PD charge pump and between 1.6 µA and 24 µA for the FD charge pump. The loop filter capacitor is fixed and has a capacitance of 500 pF. In a typical situation, the FD charge pump current is programmed significantly higher than the PD charge pump current. That larger current is needed to make the loop lock easier. This is equivalent to increasing the loop bandwidth in a linear PLL to make it lock easier. On the contrary, a small PD current is typically required so as to not inject too much charge in the loop filter every time a decision is made and thus introduce significant jitter.

5 Measurement results

The layout view of the presented eCDR is shown in figure 5. The area of the full circuit is 930 µm by 425 µm. Since the eCDR is intended to be used as a building block in a larger design, no bond pads or protection structures are included in this area. The design has been realized in a standard 130 nm CMOS process and is able to operate between $-30^\circ\text{C}$ and $100^\circ\text{C}$ with a supply voltage between 1.2 V and 1.5 V. The power consumption of the eCDR at a supply voltage of 1.5 V is between 28.5 mW and 34.5 mW depending on the number of VCO phases that is used in the phase shifter.

The internal calibration system should bring the VCO to the required 320 MHz oscillation frequency where it needs to remain stable over temperature and supply voltage variations. The trim-resistor in the Wien bridge can only be used to tune the VCO frequency at a particular temperature and supply voltage during the setup of the system. Once the circuit is in operation, the
trim-resistor cannot be changed any more while the temperature and supply voltage obviously can and will change. Both dependencies of the calibrated frequency have been characterized and are shown in figure 6. As can be seen in figure 6(a), the temperature stability is excellent since the calibrated frequency only changes less than 0.5% over a temperature range of 120°C. On top of this, the calibrated VCO frequency is basically independent on the supply voltage as can be seen in figure 6(b). The FD in the eCDR with its acquisition range of ±25% of the data rate is therefore more than capable enough to make sure that the eCDR can lock.

Once the VCO is calibrated, with an external clock or with the internal calibration system, the CDR loop can be closed and data can be applied. The extracted clock and data have been measured and analyzed at all possible data rates and with different settings for the charge pump current and the loop filter resistance. The measured RMS and peak-to-peak (PTP) jitter of the extracted clocks is summarized in table 1. It can be noticed that the jitter is higher for lower data rates. This is as expected due to the bang-bang nature of the PD that sinks or sources current during the full bit interval. Consequently, a longer bit internal results in a larger variation of the control voltage and thus more jitter. The jitter values in table 1 are valid for the data rate clocks, so 320MHz for a bit rate of 320Mbit/s for example. As mentioned previously, the other clocks are also generated, regardless of the data rate. These clocks have basically the same jitter performance as the data rate clock.

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**Figure 6.** Variation of the calibrated VCO frequency as a function of temperature and supply voltage.

**Table 1.** Jitter of the extracted clocks at all allowable data rates.

<table>
<thead>
<tr>
<th>Data Rate</th>
<th>RMS Jitter</th>
<th>PTP Jitter</th>
</tr>
</thead>
<tbody>
<tr>
<td>40 Mbit/s</td>
<td>23.39 ps</td>
<td>130.9 ps</td>
</tr>
<tr>
<td>80 Mbit/s</td>
<td>16.93 ps</td>
<td>103.6 ps</td>
</tr>
<tr>
<td>160 Mbit/s</td>
<td>10.19 ps</td>
<td>63.6 ps</td>
</tr>
<tr>
<td>320 Mbit/s</td>
<td>8.98 ps</td>
<td>58.2 ps</td>
</tr>
</tbody>
</table>
6 Conclusion

The eCDR has been presented which is intended to be implemented on the detector front-end ASICs that need to communicate with the GBTX by means of e-links. The programmable CDR accepts data at 40, 80, 160 or 320 Mbit/s and generates retimed data as well as 40, 80, 160 and 320 MHz clocks that are aligned to the retimed data. Moreover, all the outputs have a programmable phase with a resolution of 195 ps. The radiation-hard design, integrated in a 130 nm CMOS technology, operates at a supply voltage between 1.2 V and 1.5 V and consumes between 28.5 mW and 34.5 mW. A very low RMS jitter below 10 ps has been achieved and the temperature and supply voltage stability has been proven to be excellent.

References