M10.6.2: Design and manufacturing of the AMC modules with fast analogue and digital IO (at least 100 Ms/s, 14 b)

Jezynski, T (DESY)

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MILESTONE REPORT

DESIGN AND MANUFACTURING OF THE AMC MODULES WITH FAST ANALOGUE AND DIGITAL IO (AT LEAST 100 Ms/s, 14 B)

MILESTONE: M10.6.2

Abstract:

In the uTCA based LLRF system the input signals will be processed by AMC plug-in modules hosted by uTCA crate providing communication for the system components and supporting signal processing by the controller board equipped with FPGAs and DSPs. The AMC plug-in modules with ADCs and some other IO interfaces must be developed, manufactured and characterized.
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<tr>
<th>Name</th>
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<tbody>
<tr>
<td>Authored by</td>
<td>T. Jezynski</td>
<td>[DESY]   07/10/2011</td>
</tr>
<tr>
<td>Reviewed by</td>
<td>M. Grecki</td>
<td>[DESY]   10/10/2011</td>
</tr>
<tr>
<td>Approved by</td>
<td>Steering Committee</td>
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INTRODUCTION

The ADCs are a part of frontend to digital signal processing realizes by the LLRF system. For sampling of downconverted signals a high speed ADCs are needed. Due to the high number of simultaneously processed channel the ADC board must integrate several ADCs together with “glueing” logic, clock and timing inputs, communication channels and possibly additional input-output ports. The big attention must be paid to the low latency of data sampling, processing and transmission.

The main part of the LLRF system is placed in the uTCA crate hosting the controller board, several ADC boards with analogue frontends and few other components like CPU, timing, interlock boards and other boards (Figure 1). Special attention was paid to separate the noisy components (power supplies and digital electronics) from the analogue signals.

![Figure 1. Front view of the uTCA crate](image)

The signals are supplied to the ADC AMC module through the RTM module carrying downconverters (Figure 2). All communication between ADC board and controller board is handled through uTCA backplane. Another backplane (RF) is used to distribute in the crate the RF signals, clocks and timings.

![Figure 2. AMC connected to the RTM](image)
SPECIFICATION

The SIS 8300 board was developed in co-operation with Struck Innovation Systeme GmbH. It has following features:

- Double size μTCA
- Xilinx Virtex 5 FPGA
- DDR2 Memory Interface
- 4 x 1 GBit default DDR2 memory
- Atmega128 IPMI
- External Clock and Trigger Inputs
- Frontpanel digital I/O (4in/4 out) on Harlink Connectors
- RTM ADC Analog Inputs, I2C-Bus
- 10 ADC Channels 125MS/s, 16-Bit with selectable AC and DC inputs
- 2 DAC Channels 125MS/s, 16-Bit
- Clock distribution with phase shifting
- 4 M-LVDS μTCA Ports
- 2 μTCA Clocks

The following communication links are implemented on the SIS8300 module:

1. JTAG
2. PCIeExpress - 4 Lane PCI Express Interface
3. Dual SFP Card Cage for optional Multi Gigabit Link

SIS8300 BOARD BLOCK DIAGRAM

A simplified block diagram of the SIS8300 board is shown in Figure 3. The main components are: ADCs with signal conditioning circuits, processor unit (FPGA), communication links, clock distribution and IPMI controller.

Figure 3. Simplified block diagram of the SIS 8300 board
The processor unit of the SIS8300 board is based on the Xilinx Virtex5. This “User FPGA” can be programmed by JTAG connector or from the SEPROM memory. The FPGA firmware is responsible for all the functionality of the board (getting samples from ADCs, signal processing, communication, etc.). The main task of this FPGA in signal processing is to perform IQ detection on the signal samples, calibrate the signals and to send the computed values to the controller board (possibly as a vector sum from all the channels) through low latency links (LLL).

**LOW LATENCY LINKS**

The Low Latency Links to the controller board are realized by custom communication protocol (focusing on providing low latency) through the MLVDS lines on the uTCA backplane.

**PCIEXPRESS**

The SIS8300 board is also connected to the CPU board through PCIExpress interface. The purpose of this interface is to transfer a data mass to the CPU without real time regime, i.e. the typical latency (an in particular nondeterministic behavior) of the PCIExpress link is not an issue. This data may be processed by CPU to calculate system components characteristics, extract parameters and to be a source for slow feedbacks.

**IPMI**

The management code of the SIS8300 is implemented in an Atmel Atmega1281-16MU microcontroller and can be upgraded over JTAG connector.

**CLOCKS AND TRIGGER DISTRIBUTION**

The clock and trigger signals distribution schema on the SIS 8300 board is shown in Figure 4. There are various clock sources (uTCA backplane, RF backplane and front panel connectors) that can be switched by multiplexers. The FPGA and ADCs can be configured by firmware to use required clock input.
PCB PRODUCTION, ASSEMBLY AND DEBUGGING

The developed boards were manufactured and assembled. The Figure 5 shows the SIS 8300 board. The boards were tested and debugged and then used during demonstration of uTCA based LLRF system in September 2011. All the required functionalities were operating correctly. Few problems were found during the tests and corrected in the second version of the board.

Figure 5. The photograph of the manufactured SIS 8300 board

PERFORMANCE TESTS

The manufactured boards were evaluated in laboratory and during first demonstration of uTCA based LLRF system at FLASH in August-September 2011. The 1.3GHz test signal was delivered by signal generator and downconverted by downconverter board (DWC8300) and finally sampled by one of the channel on SI8300 board. The reached stability of amplitude and phase detection was 2.8e-3% and 0.004° for amplitude and phase respectively.
Short-term stability in a uTCA crate (laboratory):

Figure 6. Single channel performance of the DWC 8300 and SIS8300