Upgrade Analog Readout and Digitizing System for
ATLAS TileCal Demonstrator

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ATLAS Tile Calorimeter System

Abstract—The TileCal Demonstrator is a prototype for a
future upgrade to the ATLAS hadron calorimeter when the
Large Hadron Collider increases luminosity in year 2023. It will
be used for functionality and performance tests. The
Demonstrator has 48 channels of upgraded readout and
digitizing electronics and a new digital trigger capability, but is
backwards-compatible with the present detector system insofar
as it also provides analog trigger signals. The Demonstrator is
comprised of 4 identical mechanical mini-drawers, each equipped
with up to 12 photomultipliers (PMTs). The on-detector
electronics includes 48 Front-End Boards, each serving an
individual PMT; 4 Main Boards, each to control and digitize up
to 12 PMT signals, and 4 corresponding high-speed Daughter
Boards serving as data hubs between on-detector and off-detector
electronics. The Demonstrator is fully compatible with the
present system, accepting ATLAS triggers, timing and slow
control commands for the data acquisition, detector control, and
detector operation monitoring. We plan to insert one fully
functional Demonstrator module into the present ATLAS TileCal
detector for the LHC RUN 2 in August 2014.

Index Terms—Analog processing circuits, Circuit noise,
Pulse measurements, Analog-digital conversion, Tile Calorimeter.

I. INTRODUCTION

THE ATLAS Tile Calorimeter (TileCal) is a cylindrical
hadronic sampling detector with steel absorbers and
scintillating plastic tiles, surrounding the EM calorimeter
cryostat. It consists of a 6-meter-long central barrel
(consisting of two 3-meter-long half barrels) covering the
rapidity range |η| < 1.0, and two 3-meter-long “extended
barrel” detectors covering 0.8 < |η| < 1.7. Each barrel is
segmented azimuthally into 64 modules. The on-detector
electronics of each barrel segment is housed in mechanical
“superdrawers”[1], [2]. The entire TileCal has installed a total
of 256 electronics drawers containing 9852 channels of on-
detector readout electronics and corresponding high voltage
and low voltage supplies.

The LHC Phase II Upgrade (“High Luminosity LHC”, HL-
LHC) aims to increase the LHC luminosity by a factor of 10.
This will lead to higher event rates requiring a more intelligent
trigger, and will increase the ambient radiation seen by the
electronics. The current analog trigger system will be replaced
by a fully digital Level-1 trigger. Therefore, a Demonstrator
developed to cover a slice of detector with 48 readout
channels will help understand the readout electronics and gain
field experience for the final Phase II upgrade design. In order
to build a fully functional digital trigger and readout system
for evaluation and also making them compatible with the
present analog trigger scheme, the Demonstrator electronics
has a hybrid of analog and digital triggering.

II. TILECAL DEMONSTRATOR READOUT ELECTRONICS

In LHC Run 1 the maximum instantaneous luminosity
achieved was $8 \times 10^{33}$ cm$^{-2}$s$^{-1}$. For Run 2 in 2015, the luminosity
of the LHC will increase to $5-7 \times 10^{34}$ cm$^{-2}$s$^{-1}$[3]. Since the
readout electronics inside the Electronics Drawers are exposed
to radiation while the experiment is running, the increased
radiation levels and the limited component lifetime for current
electronics will eventually necessitate an upgraded design to
replace all of the readout electronics in the present TileCal [4]-
[6].

The present TileCal electronics in a drawer is shown in Fig.
1. The on-detector system consists of 9 different functional
boards with many interconnects; the new design reduces this
to 4 boards with few interconnects and a high level of
redundancy.

![Fig. 1. The present Tile Calorimeter and electronics drawers](image-url)
While there are several alternative front-end amplifier/shaper cards being considered for the Phase II upgrade, this first Demonstrator prototype will employ a redesign of the present “3-in-1” discrete component card; other options will be tested later. The Demonstrator will employ all other upgrade designs, including drawer mechanics, data digitizing and off-detector data acquisition electronics, Level-I trigger, high voltage supply distribution and PMT base, low voltage supplies, as well as detector control and calibration systems.

The Demonstrator on-detector electronics consists of 48 Front-End Boards (FEB: amplifier/shaper/calibration), but only 45 are instrumented with photomultipliers; 4 Main Boards (MB: LV/signal routing/digitization/control); and 4 Daughter Boards (DB: serialization/communication). Each MB+DB is an independent system communicating off-detector via fiber. The system is mounted on a water-cooled “minidrawer”, 4 of which are connected mechanically to form a complete barrel superdrawer. All communication to the off-detector readout (sROD) module is handled by the DB, apart from the back-compatible analog trigger signals. This includes detector data, timing (TTC) for synchronizing the digitizers, slow control commands, and configuration of the readout electronics, such as charge injection calibration for the on-detector electronics and Cesium source calibration for the detector and PMTs [7]. The Demonstrator will simultaneously provide the conventional analog trigger as well as the data from all cells to study digital triggers. Fig. 2 shows the readout electronics diagram for one of 4 mini drawers used in one Demonstrator detector module.

![Fig. 2. Diagram of readout electronics in a drawer (One of four mini drawer is shown)](image)

A. Analog Front-End Readout Board

Three different analog Front-End Boards are under development by three institutions.

Option-I is a board consisting of a passive 7-pole LC shaper and bi-gain amplifiers for fast signal processing and a slow integrator for radioactive source calibration and monitoring of “minimum bias event” current. The low gain and high gain amplifiers have a gain ratio of 32, each followed by a 12-bit ADC, covering a dynamic range of 17 bits [8]. This board was developed by the University of Chicago and is similar to the one they designed for the current system; it is used in the Demonstrator since it is the only alternative that can deliver an analog trigger. However, this analog trigger is not needed in the final Phase-II system.

Option-II is developed by Laboratoire de Physique Corpusculaire de Clermont-Ferrand (LPC), France. It is a custom ASIC chip, called FATALIC [9]. The chip is designed as a current conveyor, where the PMT current signal is copied to three outputs in different gains (1, 8 and 64), and each output will be followed by an external 12-bit ADC to cover a dynamic range of 17 bits.

Option-III is a modified charge integrator and encoder (QIE [10]), developed by Argonne National Laboratory (ANL) and Fermilab. The QIE consists of 23 current splitters; it gives 4 different dynamic ranges (16/23, 4/23, 2/23 and 1/23), each range has a gated integrator and a 6 bit flash ADC. The four ranges cover a dynamic range of 17 bits.

The Demonstrator analog Front-End Board has a dimension of 70mm x 47mm and sits inside the PMT block. Fig. 3 shows the diagram of this board. The analog signal processing is divided into three parts: a fast signal processing including a 7-pole LC shaper and bi-gain amplifiers, a slow signal processing including a slow integrator with 5 programmable gain settings, and a charge injection for electronic calibration.

The 17-bit dynamic range is achieved by using a high sensitivity shaper and a pair of bi-gain amplifiers with a total gain ratio of 32, along with two 40Msps 12-bit sampling ADCs. The bi-gain amplifier output signals are digitized in parallel simultaneously. With this system, a particle that has minimal energy deposition in a detector cell (e.g. a 220 MeV muon) will yield about 10 to 35 counts from a single PMT output, but each cell is viewed by 2 PMTs.

![Fig. 3. Diagram of the analog Front-End Board](image)
 proton-proton collision is essential. The Demonstrator Front-End Board uses a slow integrator to integrate the minimal bias current from each PMT and digitized by a 16-bit ADC. The other functionality of the integrator is to check the gain of each scintillator cell. This task is done by using a radioactive cesium source that travels through a hole in the scintillating tiles of the calorimeter cells [7].

B. Main Board

At present, the digitized data are stored in pipeline buffers on a digitizer board and only read out if the event is accepted by the Level-1 trigger based on analog sums of Tile towers [11], [12]. The HL-LHC will require more sophisticated algorithms requiring more detailed information. All raw data from each PMT are directly sent to the off-detector electronics for further trigger processing and data acquisition. Each Demonstrator Main Board has the data digitizers for 12 PMTs, including 12 channels of low gain and 12 channels of high gain signals from the Front-End Boards.

The phase of the sampling clocks can be adjusted by FPGAs on the Main Board to compensate the geometrical analog signal delays from the PMTs. Each FPGA on the Main Board will directly communicate with the Daughter Board via its dedicated SPI interface.

The design of the Main Board for the Demonstrator contains commercially available off-the-shelf components. Each bi-gain fast signal pair is parallel digitized by a dual 12-bit 40 Msp/s ADC (LTC2264-12). The two channels are sent out to the Daughter Board via a two bit serial bus at a speed of 560 Mbps (14 bit x 40 Msp/s). Each data word is aligned by a data clock (280MHz) and a data frame clock (40MHz). The ADC has an analog input dynamic range of 1V peak to peak. For achieving a proper DC bias for input dynamic range and adjusting the offset of baseline shifting caused by capacitive coupling, each ADC channel implements two 12-bit DACs, which allow setting the input dynamic range.

The integrator output of each analog Front-End Board is digitized by a 50 kHz 16-bit ADC, and the 3 integrator ADCs in a section can be readout by an I2C bus. A readout rate of a few kHz will be sufficient. The diagram of one channel of PMT data flow on the Main Board is shown in Fig. 4.

In order to reduce data latency and minimize the effect of single event upsets in the FPGA due to ambient radiation, all the ADC output data will be directly routed to Daughter Board without buffering in FPGAs on the Main Board, and this also results in lower latency for triggering.

Fig. 5 shows the first prototype of the Main Board. It measures 690 mm x100 mm. In order to reduce the possible failures caused by low voltage supply trips, the Main Board layout is physically divided as two regions. Functionally, the two regions are operating independently.

![Fig. 5. The Main Board for the Demonstrator.](image)

Each region of a Main Board takes its own single +10V input supply from the patch panel of the drawer and regulates down to 9 different low voltage values used by the Front-End Board, Main Board and Daughter Board electronics. The on-board diode-OR circuit for two +10V input supplies provide redundancy for the on-detector electronics; if one +10V feed fails, the other +10V supply will take over automatically. All local low voltage values for the on-detector electronics can be continuously monitored by the Daughter Board with its embedded ADCs in the Kintex 7 FPGAs.

The Tile barrel steel provides good radiation shielding, except at the exposed “near” ends where the LV power bricks are located. To enhance the radiation tolerance, the point of load regulators are all laid out in the far-end of the Main Board, where the radiation is significantly reduced. All the regulator chips have thermal sinks mounted on the back side of the printed circuit board (PCB), where we can attach thermal pads conducting the heat from the devices directly to the water cooled drawer frame.

The PCB layout of the Main Board is very challenging since it is a very long and narrow board with mixed signals. Less than 1 count rms noise can be tolerated in the 12-bit ADCs, and the 24 channels of digitized data are required to transmit at a speed of 560 Mbps to a 400-pin interconnector interfaces to the Daughter Board. In addition, there are more than 10 channels of DC/DC switchers mounted on the board, which generate switching noise on the board. A good local isolation between analog and digital signals return paths is crucial to stop grounding bounce. Therefore, careful consideration was given to the layout of the MB to preserve the analog and digital signal integrity. Switching phases of the DC/DC switches were balanced to minimize the switching noise. The PCB is laid out in 6 signal layers and 8 power layers, and 3 redundant non-split ground layers are used for achieving better signal integrity for fast analog and digital signals.

C. Daughter Board

The Daughter Board (DB), developed at Stockholm University, is a key component responsible for the multi gigabit data communication with the off-detector as well as for controlling and monitoring of all the on-detector electronics.
This board employs two Kintex7 FPGAs and two QSFP+ modules for high speed data communication to the off-detector ReadOutDevice. The data link allows reception of a 4.8 Gbps data stream encoded with the GBT protocol and transmitting data with either 5 Gbps or 10 Gbps which can be received without losing synchronization with the 40 MHz LHC clock. To prevent or deal with system failures and SEUs, the Daughter Board employs forward error correction, redundancy in the data stream, and each Kintex7 has the ability to take over the functions of the other FPGA on the board; separate QSFP+ fiber links are dedicated to each side of the DB and MB. All communications to the on-detector electronics are routed through the DB. Given the high bandwidth, the DB has been put on high speed PCB material and mounted onto the Main Board as a mezzanine card; connections between MB and DB are made via a 400-pin FMC connector.

To qualify for insertion into the current ATLAS detector, the hardware as well as the firmware has to be thoroughly tested, verified and proven to be sufficiently radiation tolerant. The hardware features of the third generation of the Daughter Board have now been tested and verified, including the electrical characterization of the gigabit transceiver performance at 10 Gbps. Using this communication framework, on-board loopback tests with different setups were performed using two different custom evaluation boards. The third prototype Daughter Board is shown in Fig. 6.

Fig. 6. The Daughter Board for the Demonstrator.

III. THE TELCAL DEMONSTRATOR SYSTEM TESTS

Main Board and Daughter Board tests started in fall 2013. The firmware of the Main Board and Daughter Board are currently under test. The sROD will be available for test in May 2014. Fig. 7 shows a prototyping test system of one minidrawer of the Demonstrator.

Fig. 7. One minidrawer of the Demonstrator.

IV. SUMMARY

Aiming to design a new readout and data acquisition system for Phase II TileCal upgrade, a Demonstrator has been built with completely re-designed electronics and mechanicals. This Demonstrator will be used to perform functionality and performance tests as the first prototype module inserted into the TileCal detector in August 2014. The readout and digitizing system employ commercially available off-the-shelf, advanced deep-micron components. The system has 17-bit linear dynamic range with a good signal-to-noise ratio for the readout of PMT signals. It is capable of forming both analog and fully digital L1Calo triggers simultaneously. The goal to build a Demonstrator is to understand the design challenges in the future Phase II upgrade and gain field experience, including the low noise readout front-end electronics design, very high speed data transmission, precise and low jitter timing implementations, as well as digital triggering algorithm evaluations.

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