A VERSATILE CABLE AND CONNECTOR ASSEMBLY
TESTING APPARATUS (NP 2026)

K. Harrison
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K. Harrison

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ABSTRACT

Detailed circuit descriptions, drawings, and photographs are given of a solid-state apparatus developed to test cable or wiring assemblies, with a maximum capacity of 244 individual conductors. Intermittent or permanent faults of either open- or short-circuit conditions are displayed. The apparatus, housed in a standard CERN chassis, accepts standard adapter plug-in units, which are easily constructed for use with almost any type of connector.
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1. **INTRODUCTION AND HISTORY**

   During the years 1969 and 1970 it became increasingly apparent that an apparatus capable of testing a multiconductor cable, or wiring assembly, was required, owing to the ever-rising number of individual cables used in spark chamber experiments.

   This report concerns the development and final versions of such an apparatus, which is capable of testing serially any cable assembly up to a maximum of 244 conductors in approximately 0.25 second; not only from a continuity point of view, but also for the detection of any short circuit between any two or more conductors.

   The original version, capable of testing up to 72 conductors, was constructed with relays; hence it had the disadvantages of being slow, costly, noisy, and lacking in reliability, but at least it proved itself to be a viable proposition, being in more or less constant use over a period of several months.

   During that period the availability of TTL integrated circuits led to the development and construction of a solid-state, purely electronic version with a 132-conductor capacity.

2. **PRESENT SYSTEM**

   The apparatus (CERN NP 2026) to be described here in detail is a further version of the above-mentioned system, with the following improvements:

   a) the cost per conductor is lower;

   b) it is easily modified for different connectors;

   c) there is greater testing capacity;

   d) it has a low-voltage fault storage read-out system;

   e) there is the possibility of continuous recycle operation for intermittent fault detection;

   f) it weighs less and is smaller in size;

   g) it is easily adaptable for a printer connection.

2.1 **Specifications**

   Dimensions: 49 x 52 x 30 cm in instrument case Implan 506 19/19

   Power : 220 V a.c. mains 100 W

   Capacity : 244 conductors maximum

   Max. resistance for open-circuit detection: 10 kΩ

   Max. resistance for short-circuit detection: 1.5 kΩ.

2.2 **Modes of operation**

   a) Automatic.


   c) Continuous Recycle in Automatic Mode for intermittent fault detection.

   d) Continuous Recycle with fault suppression for autonomous testing and internal timing adjustments.
Continuous Recycle with open-circuit fault suppression for spark chamber short-circuit or broken-wire detection.

2.3 Detailed circuit description

The circuit is described under the following six different headings:

1) Master clock and control logic.
2) Wire-under-test register and BCD decimal decoding.
3) Wire test circuits.
4) Fault detection and fault registers.
5) Reset.
6) Cold start.

Note Positive logic is used throughout in the following descriptions.

2.3.1 Master clock and control logic

The self-starting astable oscillator (T1 + T2) or the Manual Advance circuit, supply clock pulses to block S1, via blocks S4 and S5 depending on the position of the Manual/Auto switch S3.

If either Start (S1) or Recycle (S2) has been depressed, block S3 will be preset and hence Q will be high. Clock pulses will therefore appear at 1A/10 to advance the wire-under-test register, and a delayed strobe pulse STRB is applied to block 38 via the monostables block 47.

These pulses are inhibited if Overflow, OVERFLW, is low or Register Overflow S5 is depressed.

The START lamp flashes if block S3 is not preset.

The Register Overflow lamp flashes if OVERFLW is low.

Although, as mentioned above, either START or RECYCLE buttons will preset block S3, only Start (S1) will supply an Advance Cable Register pulse, ADV CBL RGS, to the register comprising BCD counters blocks 56 to 59.

Note that the clock oscillator T1 + T2 is stopped by T18 as block S3 is cleared.

2.3.2 Wire under test (WUT) and decoding

The three BCD counters 80, 81, and 82 on card 11 are advanced by each ADV WUT pulse, and the BCD outputs are decoded by cards 9, 11, 12, and 13 to give 250 outputs which consecutively go low as the register advances. The output equivalent to wire 'zero' is not used by the wire test circuits.

2.3.3 Wire test circuit

Note that

i) Inverter B and two input NAND gates C and D are open collector output.

ii) Rc is the collector pull-up resistor for inverter B.
iii) $R_b$ is the input pull-down resistor for gate D, and must be less than 470 $\Omega$ for a TTL gate to assure a valid low input.

When a $\overline{WT}$ (wire test) pulse is applied to input 1, it can be seen that $\overline{GTA}$ and $\overline{GTB}$ are active low if points 2 and 3 are connected (by the wire under test).

In the case of no connection between points 2 and 3, the base resistor $R_a$ holds the emitter low and $\overline{GTB}$ remains high.

In the case of a short circuit between the wire under test and any other wire, the points 2 and 3 will be held low by the short circuit and therefore both $\overline{GTA}$ and $\overline{GTB}$ will remain high.

Twenty-five such identical circuits are found on each test-wire card, with all the open collector points $\overline{GTA}$ connected and all the open collector points $\overline{GTB}$ connected to form two 25-input OR gates. The common collector pull-up resistor for each gate is found on control card 10.

Note that in the absence of a $\overline{WT}$ pulse because of, say, a decoding fault, $\overline{GTA}$ and $\overline{GTB}$ will stay high and thus the circuit is self-testing.

2.5.4a Fault detection Logic

Owing to fan-out limitations, only 25 gates with one common pull-up resistor are connected together; thus blocks 84 to 87 inclusive form two 250-input NOR gates followed by inverters, block 39, to give the two signals, Gate A ($\overline{GTA}$) and Gate B ($\overline{GTB}$). These signals are transformed by blocks 38, 41, and 42 into the three gated signals, Load Short Circuit (LD SC), Load Open Circuit (LD OC), and Fault ($\overline{FLT}$), which are gated by Inhibit Load (INHIBT LD) from block 40.

Note that $\overline{OK}$, block 38 pin 6, is not gated but all four above-mentioned signals are strobed by $\overline{STRO}$ to eliminate edge spikes as the decoding of the wire-under-test register takes place.

Visual fault indication is given by the FAULT lamp, because of a preset of block 45. Stop Alarm clears this bistable.

Indication is given if
i) $\overline{FLT}$ on block 41, pin 5, goes low.

ii) The final wire number is different from the number of wires in the assembly under test.

When the fault-under-test register reaches the BCD-coded final wire number, the comparator (blocks 80, 81, and 82) sends $\overline{COMP}$ to trigger monostable 40, and thus inhibits any fault loading (INHIBT LD) during the time taken for approximately four clock pulses. If, however, the ungated $\overline{OK}$ signal goes low during this time, fault indication is given, since the final wire number is set to a figure less than the number of wires in the assembly under test.

If set to a higher number, the wires will be loaded in the fault register normally, as described below.
2.3.4b Fault Loading

Either LD SC or LD OC when active will give FLT, which will advance counter 13 and
BCD counter blocks 12 and 11 (fault total register). For the first fault found, either
block 16 or 18 will be preset because of the combination of LD OC or LD SC and the decoded
'I' signal on blocks 7 and 8, pins 2. Luminous diode LD1 (open circuit) or LD2 (short
circuit) will be activated. At the same time either flip-flop will turn on T20 to apply
+Vcc to the fault 1 indicator FIH.FIT.FIU, and a short ENABLE pulse from block 3 will load
into the indicator the BCD number available in the wire-under-test register. When ENABLE
goes high this number will be stored, irrespective of changes in input data, until the
corresponding flip-flop is reset.

The next fault found will activate Fault indicator 2 by T21 and block 4, since
counter 13 and decoder 14 will advance again.

When and if a total of four faults has been found, block 13 resets itself to zero and
presets the Fault Overflow flip-flop block 53, thus giving visual indication via T24 and
stopping further clock pulses; the wire under test advances by driving block 51 pin 9
low, i.e. REC OVF53N from block 53 pin 8.

No further advance of the wire-under-test register will occur until the overflow sig-

a) Register Overflow S5, or

b) Fault Reset S7, or

c) Main Reset S6.

The switch S8, Inhibit Load, is used during test procedures to allow uninterrupted
operation of the instrument during timing adjustment.

2.3.5 Reset

As stated above, the Fault Overflow Reset button is illuminated only when four differ-
ent faults have been located and loaded into the fault indicators.

In this case and when the wire under test is any number but zero, i.e. before a test
has begun, the Fault Reset and Main Reset buttons are illuminated by block 48 and T11.

Note Main Reset will put the cable counter to zero and Fault Reset will not.

Oscillator T5 + T6, divided by counters 90 to 92 inclusive, supplies the phase-
displaced flash signals FLS 1 and FLS 2 and the two-tone audio alarm signal (emitter-followed
to the loudspeaker by T9 and T8).

2.3.6 Cold Start

Switching on the instrument gives a 2-second delay before C5 charges to Vcc by R80,
and applies Main Reset from the normally closed RL 1 contact which sets all registers to
zero and stops the clock by clearing flip-flop 53.
2.4 Continuous recycle

The rear panel switch S8 provides the possibility of continuous operation, assuming faultless operation, by allowing each RESET at the final wire number to provide RESTART on block 51 pin 2.

Any intermittent fault may thus be discovered by simply moving the cable assembly relative to the fixed panel socket in recycle mode during several seconds.

Note that any permanent fault thus found in this mode will only allow either four cycles for open-circuit condition, or two cycles for short-circuit condition due to a register overload. The same fault wire numbers will be loaded into consecutive fault indicators during each full cycle.

2.5 System disadvantages

As the system has been designed as a rapid, effective means of discovering basically human errors, it does not, under any circumstances, test the assembly from either a high voltage (i.e. insulation resistance), or high current (i.e. conductance) point of view. The limiting parameters for fault detection can be changed over a limited field, however, by modifying the wire test circuit resistor values.

Owing to the quantity of integrated circuits used, the power supply for such a TTL system must be capable of delivering at least 7 A at the standard 5 V Vcc supply voltage, resulting in a moderately large power supply.

3. SUGGESTED IMPROVEMENTS

Whilst system improvements are obviously many and varied, it is evident that use of complementary Metal Oxide Silicon (MOS) or Hi/NIL (High Noise Immunity Logic) integrated circuits, especially if developed in sufficient quantities for a production series of the apparatus as MSI (Medium-Scale Integration) or even LSI (Large-Scale Integration), would significantly decrease the power consumption and hence weight, size, and eventually cost, of the instrument.

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A Type-3 Female Adaptor Unit

A Type-3 Male Adaptor Unit
A Type-1 Printed Circuit Adaptor Unit

View of the WACO244H005 Connector representing the maximum testing capacity of 244 individual conductors
One of the ten Wire Test Cards used in the apparatus

One of the 4 Binary Coded Decimal-to-Decimal Decoders