A GENERAL-PURPOSE AMPLIFIER AND READ-OUT SYSTEM
FOR MULTIWIRE PROPORTIONAL CHAMBERS

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GENEVA
1974
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SUMMARY

An amplifier and read-out system for multiwire proportional chambers is described. It consists of the following elements: preamplifiers; receiver, trigger, and memory modules; proportional system encoder; a powered crate; and wire chamber interfaces. The preamplifiers are mounted directly on the chamber, from which signals are sent via twisted pair cables to the receiver, trigger, and memory modules, housed in crates in the experimenters' hut. Each crate contains a proportional system encoder which codes and transmits the data from up to 22 receiver, trigger, and memory modules (352 wires), after a request from the wire chamber interface. The latter module can handle information from up to eight systems of 4096 wires (32,768 wires). The input sensitivity is nominally 2.4 μA. The minimum fast strobe width is 10 nsec. The time slewing and the delay dispersion, etc., are small; thus full advantage can be taken of the intrinsic resolving time of multiwire proportional chambers when using the system.
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1. INTRODUCTION

Multiwire proportional chambers (MWPC)\textsuperscript{1)} have become a well-established tool in high-energy physics experiments. The electronics for recording signals from these chambers can be realized in different ways. In general a complete processing chain is being used for each individual wire\textsuperscript{2-20)}, but also delay lines have been applied for temporary storage of signals from many wires\textsuperscript{21-24), in order to reduce the volume of the electronics.\textsuperscript{25)}

The complete processing chain has to perform a number of defined functions. The physical layout of this chain can be organized to best suit the nature of the experiment, taking into account factors such as: accessibility, number of wires, particle rates and required system resolving times, flexibility and interchangeability, etc. Roughly speaking one has the following possible schemes:

a) Complete processing circuit mounted directly on chamber (amplifier, delay trigger, and memory). Read-out of the wire memories of each chamber is done sequentially in a parallel or serial manner through a common system data cable. This scheme is recommended for large systems \((> 5\ K\ wires)\) and lends itself well for construction in hybrid or monolithic form\textsuperscript{7,12-14,17,26}. Access to electronics during running of the experiment is limited.

b) Amplifier and trigger on chamber. The standardized signals from the triggers are sent via twisted pair cables to the memories, which are located in crates in the experimenters' hut. The cable provides the delay. This arrangement finds application in case of high rates and short resolving times.

c) Preamplifier on chamber. The non-standardized signal is sent via twisted pair cables to delay triggers and memories, which are located in crates in the experimenters' hut. In this case the delay can also be provided by the cables. This layout has the minimum amount of electronics on the chamber and the maximum within reach of the user. It is thought to be the most flexible and accessible arrangement for a small to medium number of wires \((< 5\ K)\).

The system described in the following is as mentioned under (c). An effort has been made to make a flexible general-purpose design, and not something dedicated to a particular experiment. It is constructed in modular form, grouping together the electronics of 16 wires. It can be used for chambers of all practical dimensions, can easily be expanded, and provides all essential facilities. A view of a chamber\textsuperscript{25)} equipped with preamplifiers is shown in Fig. 1. A crate with the various modules is given in Fig. 2.

2. SYSTEM CONFIGURATION

A functional layout of the system is given in Fig. 3.

The wire signal is amplified by a preamplifier, which is situated directly on the chamber. A twisted pair cable carries the output signal of this preamplifier to a receiver-trigger-memory module (RTM), where the signal is further amplified, delayed, and, in case of a valid event, strobed into a memory.

The Fast-OR (FOR) (in time with leading edge of signal) and Majority (MAJ) (real-time signal indicating multiplicity) outputs may be used to make up the event decision. As these
signals are available from each RTM module (group of 16 wires) they offer the possibility of rather refined event selection. Each module also has a separate memory Strobe input and a Flag switch which can set a bit permanently to mark that this module handles signals from the first 16 wires of a chamber.

One crate contains up to 22 RTM modules (332 wires), 1 proportional system encoder (PSE), and 1 control unit (CU). The conversation between the RTM, PSE, and CU takes place via the rear connector dataway.

The PSE will allocate a binary number -- based on channel number in module, module number in system, and system number in experiment -- to the wire that has been hit, and transfer this word through CAMAC to a computer or other storage device. The action of the PSE is initiated from the wire chamber interface (WCI). It will sense if in the RTM modules any of the memories have been set, by checking the state of the Memory-OR (MOR) output from each individual module. Only the modules that contain information will be addressed and read out in sequence. If no information is found, then the PSE in the next crate will be enabled, and so on until the last crate has been addressed.

The PSE's are "daisy chained" by a multipin front panel connector. Crates are given a number in the system from 0 to 11 by a thumbwheel switch on the front panel of the PSE. The system number is set by a thumbwheel switch on the rear of the PSE (same position for all PSE in one system). The maximum number of wires in one system is 4096.

The CU has a strobe input which is connected via the dataway to all RTM modules. This input is OR-ed in each module with the individual memory strobe inputs, and allows simultaneous strobing of all modules of a crate. A FOR output of all RTM channels present in a crate is also given by the CU.

The WCI controls the action of the PSE as already mentioned above. It generates the read-out commands and transmits the data to the CAMAC dataway and via a CAMAC-computer interface to the computer. The WCI can handle information from up to eight systems (a total of 32,768 wires).

A more simple and economic solution has also been developed, using a data input channel of an HP-2100 series computer. The conversation between the computer and the PSE's is then organized through the computer interface module. This arrangement has the additional advantage of shorter read-out time.

3. DESCRIPTION OF VARIOUS PARTS

3.1 Preamplifiers

The main purpose of the preamplifier is to convert the single-ended wire signal to a push-pull signal for the twisted-pair line going to the RTM module. In addition it gives some amplification, in order to become less sensitive to noise pick-up and to match the threshold of the RTM module.

The input impedance of the amplifier together with the series protection resistor serves as a load to the wire. In general this impedance is accepted to be 1-2 kΩ. If, however, the environment in which the chambers are going to be used is very noisy, or the chamber wires are very long, or a number of wires are grouped together on one amplifier
input, it is recommended to use a low input impedance preamplifier \( (Z_{\text{in}} = 100-200 \ \Omega) \). Also cross-talk between inputs is less with a low input impedance, though this is generally not a problem as it is overcompensated by the induced positive signals. A drawback of the low impedance preamplifier, compared to the high impedance amplifier, is the fact that more active elements are needed to obtain the same output voltage for a given input current from the wire.

The circuit which is generally being used in the system described is shown in Fig. 4a. It is a high input impedance \((Z_{\text{in}} = 1500 \ \Omega)\) preamplifier, with a rise-time of \(\approx 5.0 \ \text{nsec}\). The gain is \(\approx 10 \ \text{mV}/\mu\text{A}\). The RTM input threshold is \(24 \ \text{mV} \) (p.p.), which results in a wire input threshold of \(2.4 \ \mu\text{A} \) (or \(3.6 \ \text{mV} \) across \(1500 \ \Omega\)). Limiting of the output signal occurs at \(\approx 250 \ \text{mV} \) \((I_{\text{e.f.}} \times Z_{\text{tw.p.}} = 2.5 \ \text{mA} \times 100 \ \Omega = 250 \ \text{mV})\). One push-pull output section of an MC-1035 is being used per channel. The series protection resistor, usually \(1800 \ \Omega\), is mounted directly on the printed board of the chamber.

Originally preamplifier boards were designed to suit the number of wires of each particular chamber\(^{36}\). It soon appeared that, in general, chambers could be designed to have a number of wires equal to a multiple of 16. With this assumption, a 16-channel preamplifier board was standardized, a quantum which is also being used for the RTM modules.

A preamplifier with the same input impedance but higher gain has also been designed for chambers with low gas amplification.

A preamplifier with a low input impedance \((150 \ \Omega)\) is shown in Fig. 4b. The gain is again \(\approx 10 \ \text{mV}/\mu\text{A}\) and the rise-time \(\approx 5.0 \ \text{nsec}\), also resulting in a wire input current threshold of \(\approx 2.4 \ \mu\text{A} \) (or \(0.72 \ \text{mV} \) across \(300 \ \Omega\)). The extra section of MC-1035 is used to lower the input impedance. This preamplifier is being used on chambers where eight wires of 1 m in length are grouped to one input\(^{37}\). In this particular case much better results, from the point of view of noise pick-up, were obtained with this type of amplifier as compared to the circuit of Fig. 4a. The input protection circuit \((R1, D1, D2)\) is mounted in this case on the preamplifier board.

The twisted pair cable that is generally being used has wires with a useful cross-section of \(0.18 \ \text{mm}^2\). When this cable is long, then its attenuation noticeably increases the effective input threshold. For a length of 50 m this amounts to \(\approx 35\%\).

3.2 **Receiver, trigger, and memory modules**

3.2.1 **Receiver, trigger, and memory modules (RTM)**

The preamplified signal is received by the circuitry in the RTM module, amplified, limited, differentiated, discriminated and standardized, delayed, and stored in case of a valid event. A block diagram of one channel is given in Fig. 5. It contains the usual chain of functions. A novelty in this scheme is the feedback from the delay monostable which inhibits the input limiters. It makes the monostable pulse width (= delay) nearly independent of the input signal. It gives better performance than circuits with strong input differentiation\(^{38}\), it is more economic, and has less dead-time than a cascade of monostables\(^{18}\).

A cut-out of the complete circuit diagram showing details of one channel and a side view of an RTM module are given in Fig. 6. The complete diagram is shown in Fig. 7.
The line-receiver (MC-1035 b in Fig. 6) amplifies the signal \( \times 5 \). The standing current in the output emitter follower of this line-receiver has been reduced to 1 mA. Limiting of false (positive) wire signals to a negative pulse of 100 mV across R5 (= 180 \( \Omega \)) is thus obtained, which, after differentiation, remains below the trigger threshold of the monostable.

True (negative) wire signals are limited by D2 to a positive pulse of max. 200 mV.

The network C6 R8 differentiates weakly, to the extent that the signal is made shorter than the resolving time of the following monostable.

The monostable (MC-1035 c) is of the classic RC coupled type; it provides discrimination and delay, and has a threshold of 60 mV. The limiting and differentiating network attenuates a typical wire pulse by \( \approx 50\% \), so that finally the input threshold of an RTM channel becomes 24 mV push-pull.

The positive output pulse of the monostable is fed back via D1 to the output emitter follower of the line receiver. It cuts off this emitter follower and the limiting diode D2, so that the input signal that caused the triggering is disconnected from the monostable, and also it inhibits effectively any other input signal for the duration of the output pulse. Width variations due to input signal influence have thus been made < 1%. (The use of a diode instead of the original resistor of 68 \( \Omega \) has been suggested by Mr. J.C. Lacotte, IPN, Orsay).

The leading edge or FOR output is being obtained by simple RC differentiation (R13, C12) and fed to the module FOR circuitry (MC-1006, 17b, etc.).

The trailing edge or delayed pulse is formed by using the third section (MC-1035 a) of the integrated circuit as an active differentiator for the already weakly RC differentiated output pulse from the monostable. A well-defined narrow spike is thus obtained and fed to the memory strobe gate (MC-1010 No. 9d).

The memory (gates 9b, c) will be set when the delayed signal and strobe coincide. Its state is read through the read gate (9a). One output of the memory flip-flop is fed to the MOR gates (MC-1006, 17a, etc.). The outputs of these gates are wire OR-ed and provide the MOR signal to the rear connector. The active level is high, and occurs when a memory is set. When the Flag switch is "ON", the MOR output is permanently high and the flag bit is recorded at read-out.

The reset pulse, coming through the rear connector and a buffer (MC-1035, No. 18b), erases the memories and ends the MOR.

The module can be strobed in two ways, either individually (front panel) or together with all other modules in a crate (from CU via rear connector). The front panel strobe must be a NIM signal. It is level-shifted (T3) and OR-ed with the crate strobe, which is received in push-pull from the dataway. Four gates (MC-1047, No. 20) fan out the strobe, each to four channels.

The FOR signal is brought out on the front panel as a complementary NIM signal (optionally it can also be provided as a NIM signal by driving T1 from gate MC-1011, No. 23d). Another FOR signal is sent via two inverters (MC-1011, No. 23a and d) to the rear connector and via the dataway (two lines, of which one is being driven and the other at "Vbb") transmitted to the CU to take part in the crate FOR.
The MAJ output is a real-time signal which has an amplitude that is proportional to the number of hits that takes place during a time equal to twice the monostable pulse width. By measuring its amplitude one obtains useful information about the multiplicity -- information which can be used to make up an event decision. The circuit consists of a grounded base transistor (T2) into which a small current pulse (~1 mA) from each channel is injected in case of triggering, resulting in a step of -35 mV (across 50 Ω) at the output. The output has a d.c. bias of -150 mV in order to bring the signal into the threshold range of discriminators. The output can be used to distinguish up to seven simultaneous hits.

A variant on the above-described RTM module is shown in Fig. 8. It offers the possibility of strobing individually two groups of eight wires (1-8 and 9-16) in the module, via separate front panel inputs (T3, T4, etc.). The crate strobe from the CU will strobe all channels as before.

3.2.2 Receiver and memory module (RM)

In case of very high event rates, the limited resolving time of the delay monostable may cause counting losses and thus lead to an unacceptable system efficiency. Under those circumstances it is advisable to use the twisted pair cable as the delay element, and at the receiving end a module without any dead-time, the RM module.

A block diagram of one channel of this module is given in Fig. 9. A cut-out of the complete circuit diagram (Fig. 10), showing details of one channel, is given in Fig. 11. A d.c. trigger or Schmidt trigger (MC-1035, No. 8c) is now being used as the threshold element and to standardize the amplitude of the input signal. The threshold of this circuit is 160 mV, the gain of the line receiver (MC-1035, No. 8b) is ×5, resulting in an input sensitivity of ~32 mV push-pull. The input threshold as seen from the wire is now ~3.2 μA (or 4.8 mV across 1500 Ω). Differentiation of the input signal is not needed here, and positive wire signals are automatically rejected.

A pulse derived (by MC-1035, No. 8a) from the leading edge of the signal from the trigger, which is now the delayed pulse, is fed to the memory strobe gate (MC-1010, No. 9d). The operation of the memory is as for the RTM module.

The FOR and MAJ outputs are not available in this case, the first because the input signal to the module is already delayed and the latter because the trigger does not deliver a pulse of constant width.

Specifications of the above-described modules are summarized in Fig. 12.

3.3 Proportional system encoder (PSE)

The function of the PSE is to read out information that is present in a crate of RTM or RM modules, code the information, and send for storage, either directly or via CAMAC to the computer. In either case an interface is necessary. The PSE's are interconnected to one another and to the interface. The module contains two cards, the circuit diagrams of which are shown in Fig. 13.

A command to read the system may be given to the WCI either by an external trigger or by a software start. This command is fed to the first PSE in the chain. When the read command appears (ET) in a PSE it initiates the following cycle of operations. First it will.
load (by GATE C • CLOCK 6) the pattern of MOR information into a 22-bit register (Fig. 13a: i.c. - 14,15, ..., 24). This pattern is encoded by priority encoders (i.c. - 27,30,32), the least significant bit having the priority; thus the address of the first RTM module is established in binary form (5 bits, from i.c. - 1,28,29). The module in question is now addressed by the again decoded (i.c. - 38,39) signal to retrieve the pattern of data contained in the 16 wires and possibly a flag. This pattern is recorded (by READ GATE • CLOCK 1) in a 17-bit register in the PSE (Fig. 13b: i.c. - 3,21, ..., 24,31, ..., 34). As with the MOR pattern, this data pattern is encoded by priority encoders (i.c. - 25,35) to present the least significant data bit in binary form (4 bits from i.c. - 30). These two binary numbers, 9 bits in total, give a unique solution for a wire number within a crate. This word is transferred via the interface to the computer (through signals ENCODE (ENC) and DEVICE FLAG (DF). When a reply has been received that the word has been transferred, the least significant active bit in the wire pattern register is erased (by CLOCK 1) so that the next active bit may be encoded. If no other bit is active in the data register, the least significant active bit in the MOR register is erased (by CLOCK 6) so that the next may be encoded and thus address another module. The process continues until all modules in the crate have been read, at which time the read command will pass to the next crate. When the last crate has been read, the command returns to the WCI to indicate the end of read-out.

In order to conserve flexibility, all modules of one type are identical. Station numbers and wire numbers in each crate will thus be repeated, so a method of crate identification is necessary. This has been incorporated in the PSE in the form of an 11-position wheel switch (BOX No.) mounted on the front panel, thereby identifying the crate from the exterior. The circuitry attached to the switch is organized to add an amount to the module number, equal to the switch position multiplied by 22 (Fig. 13b: i.c. - 38, ..., 41,47,48,50, ..., 52). Thus in the first crate, numbered zero, no addition is made; in the second crate, numbered 1, the first module will become 22, and so on. This would give the system a total of 11 crates of 352 wires = 3872 wires. In order to increase this to 4096 wires (256 modules) by the use of a 12th crate, the PSE is fitted with a rear panel toggle switch (+11) so that the zero position of the wheel switch can become 12. A front panel indicator warns when this condition is selected. Each PSE also has an 8-position wheel switch (CHAIN No.) on the rear panel so that chains of crates may be labelled; thus the system may be expanded to 32,768 wires.

Conversion from ECL levels used in the RTM modules to TTL is made in the PSE (Fig. 13a and Fig. 13b: by MC-1039). All logic circuitry is made in TTL. The timing signals for the read-out process are generated by monostables (i.c. - 7, ..., 10,17,18).

The read-out time per crate may be defined as: \((1.0 + n \times t) \mu \text{sec/crate}\), where \(n = \text{number of words}\) and \(t = \text{transfer time per word to computer (2 600 nsec)}\). Since most computers require more than 600 nsec transfer time/word, time \(t\) will be dependent on computer cycle time. In the timing diagram, Fig. 14, the minimum transfer time/word is shown as 950 nsec and depends on the length of DEVICE FLAG, which can be adjusted down to a transfer time of 600 nsec/word.

The data word format and the meaning of its bits are shown in Fig. 15.
3.4 Control unit (CU)

The control unit offers the possibility of strobing all modules in a crate with a common strobe signal. It also delivers a FOR signal, which is the OR of all FOR of the individual modules in the crate.

A circuit diagram is given in Fig. 16. The "Fast strobe" is distributed by eight line-drivers (MC-1035, Nos. 1, 2, 3, 4) via the dataway to the stations in the crate. Each line-driver feeds a twisted pair, to which two or three stations are connected. The amplitude of the distributed signal is 150 mV, which is restored to MECL level by the line-receivers in the modules.

A line-receiver (MC-1035, No. 5) senses the crate FOR signal from a pair of wires on the dataway (only one side carries a signal, reception made differentially to suppress noise pick-up). An emitter follower (TL) translates the signal to NIM complementary logic level at the front panel output.

Also provided on the front panel are test points for the supply voltages and a -0.8 V output. The latter can be used as a d.c. strobe for the RM and RM modules.

3.5 Crate

A view of the crate has been given in Fig. 2. The mechanics of the crate and modules is fully compatible with CAMAC specifications (EUR 4100 and CIM 25543). However, the pin allocation of the module connector is different, and therefore a simple keying arrangement was necessary to prevent insertion of a module into a true CAMAC crate and vice versa. A power supply is plugged in from the rear, which provides 30 A at -5.2 V and 2 A at +5.0 V to the modules. The voltages are distributed via a printed circuit board, on which all module connectors are mounted. This board also serves as a dataway for the slow logic signals. The circuit diagram is shown in Fig. 17.

3.6 Interfaces

3.6.1 Wire chamber interface (WCI) (type 134)

The WCI is a general-purpose interface for the transfer of data through a CAMAC system. Single word or block transfers may be made according to the complexity of the system in use.

The unit contains the necessary CAMAC control logic, a 16-bit word buffer, etc. The logic of data transfer from the device (in this case the PSE) to the buffer is similar to that of the micro-circuit interface cards currently used in the 2100 series Hewlett-Packard computers.

The WCI is fully described in Ref. 28.

3.6.2 Computer interface (type 7524)

This interface is used only for the transfer of data to the HP computer. It uses a single micro-circuit interface card in the computer, so no control is directly available from the computer apart from the transfer conversation. External inputs and outputs are available for "Start-Read", "Reset", and "End of Read Out". Status information is given by "Busy" indicator. Data and transfer conversation pass directly to the computer, as PSE and HP dialogue are identical. A block diagram of this unit is shown in Fig. 18.
4. CONSTRUCTION AND CHECK-OUT

The construction of the various elements in the system does not pose any particular problems.

Each item is checked for proper functioning before installation. The crates, the control units (CU), the proportional system encoders (PSE), and the wire chamber interface (WCI), need verification only. Of the RTM and RM modules, a number of parameters are measured and recorded. A specially designed test box, in combination with some NIM modules, makes it possible to measure thresholds and to check out the various logic functions in a short time. The test box can activate a Delay Scanner and a Delay Unit (N-9271)\(^\text{29}\); by simple push-button operation, the delay -- from input to memory gate -- of the RTM under test can be displayed on the Delay Unit.

The RTM modules are initially wired with a timing capacity (C7) which gives a delay just below the required value. After the first delay measurement, the missing nanoseconds and corresponding capacities are defined and listed for all channels. Tolerances met are then < 5\%. The capacities (C8) are mounted and the delay is measured again, results giving a final tolerance of < 3\% (if required < 2\%).

It has been found necessary to test all twisted pair cables, not only on pin-to-pin conduction, but also to check that the pairs have been correctly grouped on the connectors. An error in this grouping results in strong cross-talk between channels, as a wire of one channel is then twisted with that of a neighbour. The way to detect possible errors is to measure the cross-talk between each pair and all the others in the cable. A special jig has been designed for this purpose.

Another test box that has been devised allows testing of complete individual wire channels and their read-out, while installed in an experimental set-up. This test box has been designed as a station of the remote-controlled system\(^\text{29}\) and can thus be operated either manually or by computer. Preamplifiers are plugged into this test box, and test signals can be injected into a selected channel or into all channels sequentially.

A number of visiting teams has been provided with the necessary documentation and advice to enable them to construct the system in their home country. The system described will also shortly be commercially available. One manufacturer already supplies individual RTM channels in thin film hybrid form.

5. PERFORMANCE

The electronics described are being used by many experimental groups around the CERN accelerators. The system has proved to be reliable, versatile, and simple to set up. The standardized modular concept allows easy interchange of equipment between groups, and its re-use after conclusion of an experiment.

A view of an experiment\(^\text{28}\) in which multiwire proportional chambers are incorporated and equipped with the described electronics, is given in Fig. 19.

A display of particle trajectories, as detected with this system, is shown in Fig. 20.
Acknowledgements

We would like to thank the CERN-Rome Group for their co-operation and most valuable comments as a first user of the system in an experiment. The stimulating discussions with our colleagues, in particular Dr. H.I. Pizer, are gratefully acknowledged.
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Fig. 1 View of some chambers equipped with preamplifiers
Fig. 2  View of a crate with various modules
Fig. 3 Functional layout
Fig. 5  Block diagram of one channel of a receiver-trigger-memory module (RTM, type 4166)
Fig. 6 Circuit diagram showing one channel and a side view of a receiver-trigger-memory module (RTM, type 4166)
Fig. 8 Circuit diagram of an RIM module with $2 \times 8$ channels (type 4177)
Fig. 9  Block diagram of receiver-memory (RM) module (type 4173)
Fig. 10 Circuit diagram of a complete RM module (type 4173)
Fig. 11  Circuit diagram showing one channel and a side view of an RM module (type 4173)
<table>
<thead>
<tr>
<th>INPUTS</th>
<th>Types 4166 and 4177</th>
<th>Types 4173</th>
</tr>
</thead>
<tbody>
<tr>
<td>Front Panel</td>
<td>1) 16 wire signal inputs (push-pull via multipin connector).&lt;br&gt;2) 1 fast strobe (NIM) for 16 RTM (4166).&lt;br&gt;2 fast strobes (NIM) for 2 × 8 RTM (4177). 1 strobe for channels 1-8.&lt;br&gt;2) 9-16 active level of strobe = 800 mV.&lt;br&gt;3) Flag switch.</td>
<td>Front Panel</td>
</tr>
<tr>
<td>Rear Connector</td>
<td>1) 1 fast strobe (crate strobe).&lt;br&gt;2) 1 Read (MECL), low level = active.&lt;br&gt;3) 1 Reset (MECL), high level = active.</td>
<td>Rear Connector</td>
</tr>
</tbody>
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<tr>
<th>OUTPUTS</th>
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<tbody>
<tr>
<td>Front Panel</td>
<td>1) 1 Fast OR (NIM), active level = 0 V.&lt;br&gt;Propagation delay from input is typically 20 nsec (at ×20 overdrive).&lt;br&gt;1) MAJ(arity).</td>
<td>Rear Connector</td>
</tr>
<tr>
<td>Rear Connector</td>
<td>1) 16 pins for data (MECL), high level = active.&lt;br&gt;2) 1 pin Memory OR (MECL), high level = active.&lt;br&gt;3) 1 pin Flag (MECL), high level = active.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Input threshold for typical wire pulses (t&lt;sub&gt;r&lt;/sub&gt; = 20 nsec, t&lt;sub&gt;f&lt;/sub&gt; = 150 nsec)</th>
<th>24 mV ± 8 mV (push-pull)</th>
<th>32 ± 10 mV (push-pull)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Threshold for positive wire pulses</td>
<td>&gt; +40 dB</td>
<td>&gt; +40 dB</td>
</tr>
<tr>
<td>Cross-talk between channels</td>
<td>&lt; -40 dB</td>
<td>&lt; -40 dB</td>
</tr>
<tr>
<td>Min. fast strobe width (≡ resolving time)</td>
<td>10 nsec. Typical values used in practice between 40-100 nsec, at full efficiency.</td>
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</tr>
<tr>
<td>MAJ(arity) output</td>
<td>No triggering: -150 mV, d.c. across 50 Ω&lt;br&gt;Step per trigger: -35 mV ± 5 mV across 50 Ω (usable up to 7 inputs)</td>
<td></td>
</tr>
<tr>
<td>Delay between input and memory gate</td>
<td>Can be chosen by timing condenser to be 100 nsec to several usec. Typical values between 150-250 nsec. Tolerance after adjustment &lt; 3% (± 2%).</td>
<td></td>
</tr>
<tr>
<td>Time slewing (of Fast-OR and delayed pulse at memory gate)</td>
<td>&lt; 10.0 nsec, for ×2 to ×10 overdrive.&lt;br&gt;4.0 nsec, for ×10 to ×100 overdrive.</td>
<td>&lt; 10 nsec, for ×2 to ×10 overdrive.&lt;br&gt;5 nsec, for ×10 to ×100 overdrive.</td>
</tr>
<tr>
<td>Resolving time (threshold recovered to &lt; 5 dB)</td>
<td>3.5 × time delay</td>
<td>No decay-time</td>
</tr>
<tr>
<td>Temperature dependence (0-60°C)&lt;br&gt;a) threshold&lt;br&gt;b) delay input memory gate)</td>
<td>&lt; 0.15/°C&lt;br&gt;&lt;0.15/°C</td>
<td>&lt; 0.15/°C&lt;br&gt;&lt;0.15/°C</td>
</tr>
<tr>
<td>Power consumption</td>
<td>1 A ± 100 mA</td>
<td>950 ± 100 mA</td>
</tr>
</tbody>
</table>

**Fig. 12** Specifications of receiver-trigger-memory (RTM) modules (types 4166 and 4177), and receiver-memory (RM) module (type 4173).
Fig. 13 Proportional system encoder (PSE), type 7225:

b) Wire and clock circuitry (card 1).
Fig. 15  Data word format
Fig. 14 Timing diagram of encoder signals
Fig. 17 Circuit diagram of powered crate
Fig. 18  Block diagram of HP computer interface (type 7224)
Fig. 19 View of some chambers equipped with the electronics described, installed in experiment R-802, at intersect 8 of the ISR.
Fig. 20 Display of the recorded information of an event. The long vertical lines are chambers; their length is proportional to the number of wires they contain and the spacing between wires. The short horizontal marks on the vertical lines indicate a detected signal. I.S.R. intersect is at left.