SOME ASPECTS OF THE MAIN RECTIFIERS FOR THE ISR MAGNETS

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Some aspects of the main rectifiers for the ISR magnets

O. Etgen, M. Groenenboom*, J. Lisser* and S. van der Meer

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The magnets of the intersecting storage rings are fed by two 6.9 MW stabilized rectifiers, each supplying a maximum of 3750 A at 1850 V. After a short general description, this report mainly deals with some aspects of these rectifiers that are new or non-standard. The most important of these are:

a) A passive filter with a current limiter that combines some advantages of damped and undamped filters.

b) A relatively small active filter of the parallel-connected type that reduces the voltage ripple to less than 100 mV.

c) An unusual thyristor gate control system, designed to combine fast, linear response with a minimum amount of subharmonics generated by firing inaccuracy.
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References
1. **GENERAL DESCRIPTION**

The most important data of the main ISR rectifiers are given in the following table.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum output power</td>
<td>6.9 MW</td>
</tr>
<tr>
<td>Maximum output voltage</td>
<td>1850 V</td>
</tr>
<tr>
<td>Maximum output current</td>
<td>3750 A</td>
</tr>
<tr>
<td>Load characteristics</td>
<td>3H, 0.45 Ω in series tap changer position</td>
</tr>
<tr>
<td></td>
<td>1/1</td>
</tr>
<tr>
<td></td>
<td>2/3</td>
</tr>
<tr>
<td></td>
<td>1/3</td>
</tr>
<tr>
<td></td>
<td>0</td>
</tr>
<tr>
<td>Current control range</td>
<td>25-100% 0-82% 0-65% 0-45</td>
</tr>
<tr>
<td>Primary voltage</td>
<td>17.8 kV $\pm \frac{5}{8}$ %</td>
</tr>
<tr>
<td>Maximum relative peak-to-peak ripple on output voltage</td>
<td>$2 \times 10^{-4}$</td>
</tr>
<tr>
<td>Maximum relative current fluctuations</td>
<td>$\pm 10^{-4}$ during 2 months $&gt; 25%$</td>
</tr>
<tr>
<td></td>
<td>$\pm 3 \times 10^{5}$ during 10 min. $&gt; 25%$ of maximum</td>
</tr>
</tbody>
</table>

The rectifiers have to supply a constant current most of the time. However, in order to provide for slow acceleration or deceleration of the stored protons, the current has to be adjustable continuously between 25% and 100% of the peak value.

This adjustment range is provided most economically by the use of diode bridges in series with thyristor bridges. The latter can work as rectifiers or as inverters ("buck-boost" system). The circuit adopted (Fig. 1) consists of two full bridges of each type, all connected in series, resulting in 12 pulse rectification throughout the control range. Opposite 7.5° phase shifting windings on the mains side of the two rectifiers ensure that the lowest harmonic in the mains current will be the 23rd if both rings are operated at the same current.
Each rectifier set is fed by two transformers in a common tank, one for the thyristor bridges and one for the diode bridges. The primary of the "diode" transformer is equipped with an off-load tap-changer that permits to choose 100%, 66%, 33% or 0% of the diode voltage. When the rectifier has to work at reduced current for a considerable time, the choice of a lower diode voltage reduces the reactive power consumption by decreasing the thyristor firing angle.

Eleven elements (diodes or thyristors) are connected in parallel in each branch of the bridges, mounted on water cooled bus bars. The circuit parameters permit working at full current with 10 elements. The fuse signalling system is designed accordingly; failure of one element will result in a warning, whereas the rectifier is switched off if two or more elements in a branch break down.

Freewheeling diodes are connected across the output in series with small resistors that will limit the short-circuit current in case of breakdown.

The rectifiers have to provide a highly ripple-free output voltage in order to allow efficient RF stacking of the protons [1]. The requirement is for a peak-to-peak ripple voltage less than $2 \times 10^{-4}$ of the DC output voltage. This specification is met by using a passive and an active filter in combination. These are described in more detail in the following paragraphs.

In order to reduce the maximum voltage to ground, the centre point of the magnet circuit is earthed. The complete rectifier circuit is therefore floating with respect to earth. The electronic circuits used for regulation and for the active filter are, however, near ground potential. This is made possible by the use of a direct current transformer [2] for current measurement, by connecting a transformer in the active filter output, and by using differential inputs for voltage feedback.
The current regulation system has been designed to cope with sudden 5% changes of mains voltage. Although such changes are rare on the 18 kV distribution system to which the rectifiers are connected, the somewhat unusual range for rectifiers of this size was needed in order to minimize the risk of losing the stored protons and having to repeat the time-consuming accumulation process.

Since rectifiers of this kind are not exceptional, the remainder of this report will mainly deal with features that are not usually found in similar installations.
2. THE PASSIVE FILTER WITH CURRENT LIMITER

It is well known that passive filters for large rectifiers must have a damped response to sudden voltage changes in order to avoid overvoltages on the filter capacitors and on the rectifier output in case of sudden voltage variations, for instance, due to sudden changes of reference voltage. This damping, unfortunately, results in a ripple attenuation much worse than that of an undamped filter.

For the ISR main rectifiers, a solution was found that combines the advantages of damped and undamped filters. As Fig. 2 shows, a simple critically damped LCR filter is adopted, with a diode bridge in parallel to the resistor \( R_1 \). The small auxiliary rectifier delivers a biasing current to this bridge that is a few times higher than the maximum ripple current. The diodes therefore act as a short-circuit on \( R_1 \), making the filter undamped for ripple current. As soon as the current through \( C_1 \) becomes larger than the auxiliary current due to sudden output voltage changes, two of the bridge diodes will block, and the filter is now damped by \( R_1 \), in parallel with the auxiliary choke \( L_2 \). The latter has to be dimensioned to keep off the voltage across \( R_1 \) during the charging of the capacitor. In the present case, \( L_2 \) weights about 5 times less than \( L_1 \).

At the fundamental ripple frequency (600 Hz), the filter is about 20 times as effective as it would be without the current limiting device. An additional advantage of this circuit is that the output of the active filter can now be connected in series with the limiting bridge, as shown in Fig. 2, so that it is protected against the high charging current that can occur during sudden output voltage changes.

The small capacitor \( C_2 \) serves to remove the small fast steps in output voltage that would otherwise occur at each thyristor firing due to the stray inductance in the current limiting circuit and in the active filter output transformer (which is of the order of 10 \( \mu \)H). Such steps
would be too fast to be removed by the active filter. \( C_3 \) and \( R_2 \) serve to damp the parallel resonance of \( C_2 \) with the stray inductance in the current limiter.

The complete equipment is floating with respect to ground, and both the passive and the active filter will only reduce the ripple voltage between the two output terminals. A relatively large ripple voltage between both terminals together and earth might still subsist due to stray capacity to earth in the a.c. part of the rectifier. In order to reduce this common-mode component, the small capacitors \( C_4 \) and \( C_5 \) are directly connected to earth. Even so, the common-mode ripple voltage is still a few times higher than the ripple between the output terminals. It has, however, little influence on ISR operation.
3. **THE ACTIVE FILTER**

The active filter used is of the parallel type; i.e. it tries to cancel the remaining ripple by feeding back a ripple voltage in series with the capacitors of the passive filter, as shown in Fig. 2.

The more usual systems of the series type require either transistors in series with the main circuit, resulting in unacceptable power loss and number of transistors, or an expensive choke or transformer in the main circuit. The solution adopted is by far the most economical. The output transformer now only has to pass the ripple current and is therefore quite small. A total of 80 conservatively rate power transistors are used in the push-pull filter output stage, which can deliver a peak sine wave power of about 1200 W.

The reason why this output power can be so low is connected with the way in which the filter is incorporated in the overall regulation system. Often an active filter is treated as a separate device that tries to keep the rectifier output constant at ripple frequencies. If a considerable ripple reduction is needed, the open loop gain of the active filter must be high, and it will then necessarily be above unity in a wide frequency range, including the range of mains voltage fluctuations. Therefore, the filter will also try to cancel the effects of mains voltage jumps. Moreover, whenever the output voltage is changed on purpose by changing the reference voltage, the active filter will oppose this and tend to be saturated. These effects rather than the ripple amplitude usually determine the size of the active filter output stage.

In the present design, the filter is not treated as a separate entity. Instead, it is an integral part of the regulation system (Fig. 3). Since the filter output commands the thyristor firing angle, any saturation tendency will be counteracted rapidly. In fact, even with sudden 5% mains voltage changes, the filter does not saturate.
It is clear that the active filter output should have a low impedance for obtaining the best passive filter performance. This is achieved by voltage feedback around the power amplifier (not shown in Fig. 3).

In order to prevent damage to the output stage if the input is saturated during switch-on or during tests, the circuit contains two limiting systems with different level and time constant that limit both the peak output current and (at a lower level) the average value.
4. ANALYSIS OF THE REGULATION SYSTEM

The following analysis will be given in terms of Bode diagrams and will therefore be valid for small-signal conditions only (i.e. no saturation anywhere). A large signal effect will be discussed in paragraph 5.

Fig. 4 shows the most important Bode diagrams. The designations at the left side of the diagrams correspond with Fig. 3; e.g. A → B refers to the transfer function \( V_B/V_A \). All curves are shifted vertically by arbitrary amounts in order to improve readability. The actual voltage gain is given in one point for each curve by a figure associated with a vertical arrow. Figures at the transition points give the transition frequencies in Hz. Sloping asymptotes are marked with a number of small dots corresponding with the order of the slope.

The auxiliary loop (dotted line in Fig. 3) will be disregarded here. Its function is explained in paragraph 5.

One of the most important points in the design of the system is the proper overlap between the thyristor regulator response and the active filter. Signals from point A are transferred to point C through two channels: the low frequencies through the thyristor regulator and the passive filter, the high frequencies through the coupling transformer and again through the passive filter, now in inverted connection. At the cross-over frequency, where these two channels have equal gain, their relative phase shift should not be too near to 180° in order to avoid cancelling of the two signals. Translated in terms of Bode diagrams, this means that in a region around the cross-over frequency the difference in slope between the two channels should not be much larger than 20 dB/decade.

Of course, it is necessary to choose a cross-over frequency as high as can be reconciled with this requirement, in order to reduce the power of the active filter output stage. In the present case, the cross-over
is at 60 Hz. This is about as high as practicable with 12 pulse rectification and a fast gate control system. Note that the transition at 150 Hz in the diagram of Fig. 4b approximates for small signals the effect of the mean delay (0.83 ms) before the next thyristor is fired.

The complicated high frequency behaviour of the passive filter response (Fig. 4e) is caused by the presence of stray reactance in various points of the filter circuit and by the presence of capacitance in parallel with the filter output. In fact, it appeared that between the active filter output and the parallel capacitors $C_2$, $C_4$ and $C_5$ (Fig. 2) sufficient stray reactance was present due to long bus bars to reduce their effect on the high frequency behaviour of the curve (Fig. 4e). However, the parallel capacity due to the earth shields on the power output cables had a considerable effect, since the voltage feedback (point C in Fig. 3) is taken directly from the output terminals. Not all of these stray effects were anticipated in the design stage, but it appeared to be easy to compensate for them by suitably shaping the frequency response of the "voltage loop" circuit (Fig. 4g and h). The complete open loop gain of the voltage loop is given by Fig. 4i. Ripple suppression is improved by the steep rise of gain below 3600 Hz, whereas stability is ensured by the shape of the curve above this frequency.

Super-imposed on this voltage loop is a current loop, as shown in Fig. 3. The cross-over between voltage regulation (mainly for ripple reduction) and current regulation is at about 3 Hz. This rather high frequency was chosen in order to obtain a good dynamic response to changes of the reference voltage. A disadvantage of a high cross-over frequency is the sensitivity of the circuit to ripple from the reference source and from the d.c. transformer and to noise in the first low-level amplifier. Because of the low voltage ripple required, this necessitated the use of a low-pass filter in the current loop. An active filter with a sharp cut-off at 30 Hz solved this problem.
The ripple voltage at the output is well below 100 mV peak-to-peak at all current settings. Most of this remaining ripple is due to parasitic effects rather than to insufficient gain of the active filter. The d.c. stability is well within specification, i.e. \( \frac{\Delta I}{I} < \pm 10^{-4} \) during 2 months and \( < \pm 3.10^{-5} \) during 10 minutes, where I is the chosen current value, between 25% and 100% of the maximum.
5. NON-LINEAR EFFECTS AND AUXILIARY FEEDBACK LOOP

Although the linear analysis shows that the system is stable for small signals, this is not necessarily the case if any part of the circuit is saturated. In fact, it can easily be seen that the system would be unstable if either the low frequency channel through the thyristor regulator or the high frequency channel through the coupling transformer would not be present. Since the power amplifier of the active filter can only supply a relatively small output signal, large oscillation amplitudes, if present, would cause it to be saturated most of the time. In fact, during model studies made before the equipment was ordered, it appeared that the circuit as described above, without the auxiliary feedback loop between points D and H could be brought into permanent oscillation by a sufficiently large perturbation.

The auxiliary loop solved this problem. This loop provides a unity gain connection between points D and H and has a negligible influence during linear operation. However, if the power amplifier saturates, it remains in action, being stable under all circumstances and providing sufficient signal to counteract the saturated power amplifier output, if necessary. It so prevents run-away of the rectifier output voltage and has the additional advantage that it permits switching off the active filter, for instance in case of a fault, without degrading the performance too much. Of course, a larger ripple voltage (up to 3 V peak-peak) will then be present.

Note, in Fig. 4n, the flat part of the curve between 7 Hz and 30 Hz, which is desirable in order to keep a sufficient phase margin just below 30 Hz despite the resonant behaviour (implying a near - 180° phase shift) of the undamped passive filter.
6. NON-SYNCHRONOUS GATE CONTROL

A non-synchronous gate control system has been described by Cassel [3]. This system works by comparing the unsmoothed d.c. voltage with a reference (Fig. 5a) and generating firing pulses whenever the rectified voltage falls below the reference value. The pulses may be distributed between the thyristors by means of a ring scaler, incremented by each firing pulse, and an associated decoder. The thyristors are fired in a fixed, pre-established order. In large rectifiers, especially if working in the inversion region, circuits that limit the firing angle must be provided in addition.

The obvious advantages of this system are its speed of response and its freedom from individual phase adjustments. The resulting absence of sub-harmonics due to firing pulse asymmetry is important when a low ripple is required.

The main drawback of the system is its non-linearity. The average d.c. output voltage is not proportional to the reference voltage; in fact, for a 6 pulse system working in the inversion region, the gain becomes infinite at a firing angle of 150°. This variable gain makes it impossible to design a regulating system with optimum speed throughout its range. Another disadvantage is its sensitivity to harmonics on the mains voltage.

Both points can be cured by a relatively simple modification. We shall first consider the effect of adding an integrating network before the discriminator (Fig. 5b). Clearly, this will ensure perfect equality of reference and average rectified voltage, since otherwise the integrator output voltage would increase or decrease indefinitely. The integrator also reduces the effect of mains harmonics.

It can be seen, however, that this arrangement is unstable. If we assume (Fig. 5c) that at a certain moment one of the firing pulses is advanced for some reason, it can be seen that the integrator will generate a sub-harmonic, because it keeps the area of each negative "triangle"
equal to that of the preceding positive one. Moreover, if a driving force for the sub-harmonic (like, for instance, mains asymmetry) is present, it can be shown that the sub-harmonic content will grow with time.

This instability can be cured in different ways. One simple method is the addition of a proportional signal to the integrated one (Fig. 5d). The amount of proportional signal caused by the resistor R is a compromise between stability and speed of response. It can be shown that optimum response is obtained by making RC equal to half the average interval between firing pulses. This method will, however, re-introduce some sensitivity to harmonics or sudden transients on the mains voltage.

A different method, adopted in the present rectifiers, is illustrated in Fig. 5e. The integrator output is now compared with a sawtooth waveform reset at each firing pulse. Since the voltage across R in Fig. 5d is also approximately a sawtooth, the system is more or less equivalent to the preceding one, except that now the sawtooth voltage is not affected by mains harmonics. Again the sawtooth amplitude is chosen as a compromise between stability and speed of response. A low sawtooth amplitude will tend to increase the sub-harmonics caused by unbalance in the mains and in the rectifier transformer (as all high-speed gate control systems do), a higher value will reduce the speed of response. A good compromise is obtained by making the peak-to-peak sawtooth amplitude about equal to the peak-to-peak amplitude of the integrator output at its maximum value (i.e. at a firing angle $\alpha = 90^\circ$).

The system that distributes the firing pulses between the thyristors is also different from the one described in [3]. In fact, a normal 12 pulse gate control system is used, working according to the well-known principle of a control voltage being compared to 12 sawtooth voltages, synchronized with the mains voltage. This system contains, as usual, the arrangements for limiting the minimum and maximum firing angles. Its input (control voltage) is normally at a value corresponding to minimum output (in this case full inversion). As soon as a firing pulse is re-
quested by the non-synchronous system described above, the input voltage rapidly (in about 80 $\mu$s) changes to the value corresponding to full output, i.e. minimum firing angle. The first sawtooth that is crossed generates a firing pulse, and the input voltage is then returned to the full inversion value. A circuit that prevents firing a particular thyristor branch more than once per period is included.

With this method good linearity and equal spacing between the 12 sawtooth voltages are not required. The intervals between the firing pulses are entirely determined by the non-synchronous circuit preceding the normal gate control unit.

An additional advantage of this method is the insensitivity to mains voltage fluctuations. In fact, if the integrator gain is infinite, mains voltage fluctuations are automatically compensated without requiring a change of control voltage. In practice, this requirement can be approximated quite closely.

The system is fairly insensitive to harmonics in the mains voltage. When both rectifiers are working at the same time there is no mutual interference with up to about 10% harmonics (Fig. 6). By changing the 18 kV mains configuration, it was possible to vary the amount of harmonics present, and it was found that mutual interference started when the harmonics content was about 1.5 times as high as in Fig. 6. This interference takes the form of sub-harmonic oscillations of both rectifiers.

Fig. 7 shows the rectified voltage before the passive filter during normal stable operation with a mains voltage as in Fig. 6. This oscil-
logram is intended as an illustration of the presence of many effects that have been omitted in the explication of the non-synchronous gate control system. Some of these effects are: mains harmonics, transformer unbalance, commutation effects, overswing on transformer secondaries
after firing, coupling between different secondary windings. Despite these chaotic effects, the system worked correctly. The typical active filter output voltage is shown in Fig. 8. This is approximately equal to the ripple that would be present on the output with the active filter switched off. It consists mainly of subharmonics, because the 600 Hz fundamental is very efficiently filtered by the undamped passive filter. With the active filter on, the output voltage ripple is typically as in Fig. 9. The sharp spikes that can just be seen at the beginning and end of each commutation contain frequencies of the order of 50 kHz and above. They are removed by a filter consisting of the inductance of two "reference magnets" [1], combined with the earth capacity of the d.c. cable system.
REFERENCES


FIG. 2: PASSIVE FILTER

FROM AUXILIARY RECTIFIER

L2 80mH

TO LOAD

OUTPUT FROM ACTIVE FILTER (LOW IMPEDANCE)

FROM RECTIFIER

L1 2 mH

R1 0.83

R2 50mΩ

C1 0.00000

C3 0.00000

C2 0.00000

C5 100μF

C4 100μF

390μF

12mF

2mF

10mF
FIG. 3: BLOCK DIAGRAM OF THE REGULATION SYSTEM

1. Passive Filter
2. Rectified Voltage
3. Thyristor Regulator
4. Coupling Transformer
5. Correcting Filter
6. Power Amplifier
7. Voltage Loop
8. Current Loop
9. Reference Voltage
10. Current Transformer
11. Load
12. Mains
13. Control Voltage
a) B→C  
PASSIVE FILTER

b) H→C  
THYRISTOR REGULATOR +  
PASSIVE FILTER

c) A→H  
CORRECTING  
FILTER

d) A→C  
LOW FREQUENCIES  
THROUGH THYR. REG.

e) A→C  
HIGH FREQUENCIES  
THROUGH COUPL. TRANSFO.

f) A→C  
TOTAL

g) D→A  
VOLTAGE LOOP  
AMPLIFIERS

h) C→K  
POTENTIOMETER

i) OPEN LOOP GAIN  
VOLTAGE LOOP

FIG 4/1:  
BODE DIAGRAMS
j) $E \rightarrow C$
WITH VOLTAGE LOOP CLOSED

k) $C \rightarrow F$
LOAD

l) $F \rightarrow E$
CURRENT LOOP AMPLIFIER

m) OPEN LOOP GAIN CURRENT LOOP

n) $H \rightarrow K$
OPEN LOOP GAIN AUXILIARY LOOP (CURRENT LOOP OPEN, ACTIVE FILTER SWITCHED OFF)

FIG 4/2:
BODE DIAGRAMS
FIG 5:
NONSYNCHRONOUS GATE CONTROL
Fig. 6 - Mains voltage with harmonics

Fig. 7 - Voltage before passive filter
(100 V/cm, 1 ms/cm)
Fig. 8 - Output voltage active filter
(1 V/cm, 2 ms/cm)

Fig. 9 - Typical rectifier output voltage
(top: 100 mV/cm, 0.5 ms/cm, bottom: 100 mV/cm, 5 ms/cm)