A LOW NOISE CMOS INTEGRATED SIGNAL PROCESSOR FOR
MULTI-ELEMENT PARTICLE DETECTORS

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ABSTRACT

A full custom chip has been built for readout of a multi-element silicon detector in the UA2 collider experiment at CERN. The low-noise performance enables the use of this chip for detecting random particles or single X-ray photons of medium energy (~ 20 keV). It can be used equally well in various other types of particle detectors which produce random signals. The noise is sufficiently low (< 0.09 fC r.m.s.) for detection of signals of ~ 0.8 fC, corresponding to 20 keV energy deposit in a silicon detector.

1. INTRODUCTION

The development of low-noise, low power ASIC for readout of random pulse signals from relatively large capacitance (1-100 pF) detector elements is essential to the construction of large area (~ 1 m²) imaging devices for ionizing radiation (single X-ray photons or elementary particles). Such imaging devices, with various pixel dimensions (20 μ m² - 1 cm²) and with fully parallel readout are required for medical imaging, synchrotron radiation experiments, space astronomy and particle physics experiments, and present a considerable number of channels (10^4 - 10^8).

Using a commercial 3 μ m n-well CMOS process, an analog signal processor has been designed for fast, low level random signals. The processor consists of a low noise charge preamplifier, a band pass filter, a track and hold stage and an analog multiplexer with the digital control (fig. 1). The analog part uses the continuous time filtering technique. The charge amplifier, POTA, uses a long channel MOS resistor as resistive feedback element. The second stage, NOTA, a pulse shaper amplifier, uses a n-well resistor as resistive feedback element.

When a particle or photon hits a detector element, a current pulse is delivered by the detector to the first amplification stage POTA. The output voltage amplitude of this charge amplifier is proportional to the integrated charge. The output pulse is filtered by the second stage NOTA. The track and hold stage stores the analog signal which is then scanned during the readout phase. A 4-channel and a 16-channel version have been produced. The digital clock lines and the analog bus can be organized in a daisy-chain configuration of 256 channels.

2. COMPARISON OF CIRCUITS USING SWITCHED CAPACITOR OR CONTINUOUS TIME FILTERING TECHNIQUE

ASIC for low noise pulse amplification of charge delivered by semiconductor radiation detectors have been implemented in recent years using switched capacitors [1-3]. A synchronous clock is used for the autozeroing of the integrator and the correlated double sampling filter. This is made possible by the repetitive character of the interactions to be registered, but it is incompatible with the readout of randomly arriving particles or single X-ray photons. Historically, continuous time filtering techniques were always used in charge amplification circuits with discrete components [4]. It therefore seems of interest to pursue the implementation of the continuous time feedback technique in CMOS integrated circuits for low noise charge amplification. Such an approach has already been proposed by Tsvividis et al. [5] for other applications. Also, for low level charge amplification, with an input signal below 3 fC, the noise performance of the continuous time feedback may be better because clock feedthrough and sampling noise from switches are factors limiting the performance of the switched capacitor technique.

3. CHARGE AMPLIFIER

The building block of the charge amplifier is conceived as a folded cascode Operational Transconductance Amplifier (POTA). It uses a single input p-channel MOS transistor with a large W/L to achieve a low noise performance, both by increasing the transconductance g_m and by reducing the flicker noise contribution. It is designed in a waffle-iron geometry to minimize parasitic capacitance and resistance of connections to source, drain and gate. The silicon detector element is a reverse biased (with V_{BIAS}) diode and is DC coupled to the input of the chip, as shown in fig. 2. This solution avoids bulky AC coupling capacitors and bias resistors on the detector or on the chip, which are in both cases not easy to implement and would consume a large chip area.

A particular problem in case of DC coupled detector elements comes from variations in the diode reverse current ("dark" current I_{dark}) which cause a DC offset and eventually saturation, because in DC the circuit is a current to voltage converter. If V_T is the threshold voltage of the input transistor, the voltage V_{OUT} at the output of the charge amplifier is given by

$$V_{OUT} = V_T - R_f I_{dark}$$

Although a typical value for I_{dark} is only 5 nA per silicon detector element, currents of up to 100-200 nA may occur. By using a long channel MOS transistor as a resistive feedback element in the loop of the charge amplifier, one can maintain the DC output level well within the dynamic range of the POTA, even for DC input currents of up to 500 nA. In spite of the non-linear DC characteristic of such a resistive feedback, the dynamic charge gain for pulse input signals is not too much degraded if the peaking time is short compared to the decay time of the output signal. It can be calculated that here this degradation is only 0.06% per nA input current, for the actual peaking time (600 ns) and the feedback capacitance of 1 pF. As shown in fig. 2, the n-channel transistor is connected across the feedback loop and biased in such a way that the source is connected to the output, and the drain to the input of the POTA stage. In this configuration the DC output voltage V_{OUT} of the POTA stage controls the bulk source voltage V_{BS} and the gate source voltage V_{GS} of this n-channel MOSFET.

$$\begin{aligned} V_{BS} &= V_{BULK} - V_{OUT} \\ V_{GS} &= V_{GATE} - V_{OUT} \end{aligned}$$

As a consequence, its conductance G becomes a function of the diode reverse current I_{dark} at the input of the POTA stage. From further analysis of this configuration a simplified expression can be obtained:

$$G = G_o + k I_{dark} = 1/R_f$$

- G_o is the value of the MOSFET conductance at $I_{dark} = 0$.
- k is a coefficient ~ 1 .

If I_{dark} increases, the conductance G increases (R_f decreases) and the DC output voltage V_{OUT} is stabilized. In the present circuit design $W/L = 3/180$ and $G_o = 30 \times 10^{-9}$ siemens which correspond to 33 M Ω , and for $I_{dark} = 100$ nA $G = 133 \times 10^{-9}$ siemens or 7.5 M Ω . For 100 nA of dark current, the penalty for this way of stabilization is measured to be a 5% decrease of the charge gain V_{out}/Q_{in} of the charge amplifier, in good correspondence with the calculated value of .06% per nA.

4. PULSE SHAPER AMPLIFIER AND TRACK AND HOLD

The pulse shaper amplifier is constructed around the building block NOTA which is also a folded cascode OTA circuit configuration using a n-channel input device to obtain a large gain bandwidth product. This filtering stage performs a differentiating function by the interstage AC coupling realised by the capacitor C_{diff} (fig. 1). This also eliminates remaining DC offset introduced by the dark current. The feedback loop of this stage consists mainly of a RC distributed n-well resistor which performs a smoothed gaussian continuous time filtering of the signal pulse. The result is shown in fig. 3.

The track and hold stores the amplitude of the output pulse at a time defined by an external trigger for retrieval by the multiplexer. This stage is the conventional circuit configuration of the sample and hold with the hold capacitor C_h (fig. 1), the switch SWH and is followed by a unity gain buffer. The unity gain buffer consists of a source follower which is matched with the NOTA stage in order to obtain an output DC offset level close to zero.

A picture of the 4 channel chip is shown in fig. 4, and fig. 5 gives the 16-channel chip mounted in its ceramic chip carrier.

PERFORMANCE

The gain of the signal processor is 10 mV/fC with < 2% non-uniformity from channel to channel. The linear dynamic range corresponds to a maximum charge of 120 fC at the input. The peaking time, which is the time from the start of the input pulse until the top of the amplitude of the gaussian pulse, is 600 ns; the track/hold charge injection is - 3 mV and the droop rate < - .1% per ms. The power dissipation is 2 mW per channel. The equivalent noise charge for zero external detector capacitance is 0.09 fC r.m.s. For 25 pF it is 0.15 fC r.m.s. This noise corresponds to 4 resp. 7 keV fwhm in silicon detector spectrometry, and is mainly determined by the flicker noise (1/f) characteristics of the input transistor in the first stage.

To evaluate the overall performance of this ASIC chip with a multi-element silicon detector, a measurement has been performed using penetrating electrons (2.3 MeV) from a ^{90}Sr β source incident on the detector. A trigger is provided by a scintillator + photomultiplier, so that only signals are registered from electrons that completely have traversed the silicon detector. Fig. 6 gives the resulting spectrum of energy deposit in the silicon detector. Full width at half maximum of the pedestal is 9 keV (0.16 fC r.m.s.) for a detector capacitance of 25 pF and a dark current of 10 nA. This value corresponds to an equivalent noise voltage of 6 μV r.m.s. The main spectral peak, which has the shape of a Landau distribution as expected, corresponds to an energy deposit of 90 keV. It is very well separated from the pedestal noise.

CONCLUSION

The first results are presented which have been obtained with a CMOS integrated signal processor for low level, random pulses, usual in various types of ionizing particle detectors (semiconductor detectors, liquid detectors, drift chambers). It is distinguished from previous circuits by the use of continuous feedback. The special feedback element allows a fairly high DC input current from a DC coupled detector element. The input transistor can be easily scaled and is designed to have low noise performance even in connection with large capacitance (200-300 pF) detector elements.

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Fig. 1 Block diagram of the 16 channel integrated signal processor.

Fig. 2 DC coupling of the Si detector elements to the inputs on the chip. The detector reverse biasing circuit is shown at the left. I_{dark} is the diode reverse current of the detector element. The feedback resistor R_f is a long channel MOSFET.

Fig. 3 Output response for a 3.5 fC input signal with 10 pF detector capacitance:
A 2 mV input pulse;
B output pulse;
C output after track and hold.

Fig. 4 Photo micrograph of 4 channel chip.

Fig. 5 Photo micrograph of 16 channel chip mounted on the ceramic chip carrier.

Fig. 6 Energy spectrum of fast electrons penetrating through a 300 μm thick Si detector. The main spectral peak (right) corresponds to 90 keV energy loss, and has the typical shape of a Landau distribution. The pedestal peak at the left is positioned around the zero-energy point, and its width is a measure of the electronics noise (9 keV fwhm).