A FIVE-CHANNEL STROBED COINCIDENCE UNIT

M. Moore and H. Verweij
Propriété littéraire et scientifique réservée pour tous les pays du monde. Ce document ne peut être reproduit ou traduit en tout ou en partie sans l'autorisation écrite du Directeur général du CERN, titulaire du droit d'auteur. Dans les cas appropriés, et s'il s'agit d'utiliser le document à des fins non commerciales, cette autorisation sera volontiers accordée.

Le CERN ne revendique pas la propriété des inventions brevetables et dessins ou modèles susceptibles de dépôt qui pourraient être décrits dans le présent document; ceux-ci peuvent être librement utilisés par les instituts de recherche, les industriels et autres intéressés. Cependant, le CERN se réserve le droit de s'opposer à toute revendication qu'un usager pourrait faire de la propriété scientifique ou industrielle de toute invention et tout dessin ou modèle décrit dans le présent document.

Literary and scientific copyrights reserved in all countries of the world. This report, or any part of it, may not be reprinted or translated without written permission of the copyright holder, the Director-General of CERN. However, permission will be freely granted for appropriate non-commercial use. If any patentable invention or registrable design is described in the report, CERN makes no claim to property rights in it but offers it for the free use of research institutions, manufacturers and others. CERN, however, may oppose any attempt by a user to claim any proprietary or patent rights in such inventions or designs as may be described in the present document.
A FIVE-CHANNEL STROBED COINCIDENCE UNIT

M. Moore and H. Verweij

G E N E V A
1971
SUMMARY

The instrument to be described contains five independent single-input channels which can be gated by a common "strobe" signal. Each channel has a front-panel switch giving the choice of making it subject to the common signal or not.

The minimum input width is 1.5 nsec and the minimum strobe width is 2 nsec. The maximum frequency of operation is at least 50 MHz with the standardized output width of 8.5 nsec and could be increased by reducing the output width. One logic and one complementary logic output are provided for each channel.

The unit, type N6236, has been designed to accept standard NIM¹) signal levels and is part of the CERN-NIM compatible nucleonic instrument range²).
CONTENTS

1. INTRODUCTION 1
2. THE INPUT AND-GATES 1
   2.1 In the ON mode 1
   2.2 In the STROB mode 1
3. THE d.c. TRIGGER CIRCUIT 2
   AND ITS CONNECTION TO THE DISCRIMINATOR CIRCUIT
4. THE DISCRIMINATOR 2
5. THE OUTPUT CIRCUIT 3
6. PERFORMANCE 3
REFERENCES 5
1. **INTRODUCTION**

An arrangement that consists of a number of twofold AND-gates having one input in common, has become known as a strobed coincidence, the common input being termed the strobe.

A circuit of this kind finds application in experiments where many counters are referred to one time signal which is produced by one or more other counters. The present instrument (Fig. 1) has been designed to operate with input and output signals conforming to the NIM/ESONE fast logic level specifications\(^1\). This implies that signals, such as those from photomultipliers, must pass via an amplitude standardizer (limiter, shaper, discriminator, etc.) before being connected to the unit.

Five independent channels are provided, each having a single input, which may be switched permanently on, or put under the control of a common strobe input. Inputs switched to STROB, only produce outputs when their signals coincide with the strobe signal.

Every channel delivers one logic and one complementary logic output which are of fixed width (8.5 nsec).

A functional block diagram of the unit is given in Fig. 2.

2. **THE INPUT AND-GATES**

2.1 **In the ON mode**

The input AND-gates consist of two diode current switches which feed into a tunnel-diode d.c. trigger circuit (Fig. 3)\(^1\). One diode pair is driven by the input signal (IN) while the other is driven from the common strobe input.

Taking the top channel of Fig. 3 as a model, \(D_1\) and \(D_6\) are a matched pair of hot-carrier diodes which, in the absence of any input signal, are each conducting \(\sim 4\) mA. Thus with the front panel switch \(S_1\) in the ON position, the tunnel-diode \(D_7\) is in the low state and conducting \(\sim 2.7\) mA. A logic signal applied to channel 1 will transfer the 4 mA from \(D_6\) into \(D_5\) and raise the tunnel-diode current by the same amount. This causes \(D_7\) to switch to the high state and a signal will be delivered to the following circuitry.

The input impedance of each channel consists of 75 \(\Omega\) (\(R_1\)) in parallel with the diode current switch \((D_3, D_4)\) and subsequent circuit. This impedance is very non-linear but gives adequate 50 \(\Omega\) matching over the input signal amplitude range of interest.

Diodes \(D_1\) to \(D_4\) provide input protection.

2.2 **In the STROB mode**

The strobe buffer is common to all channels. Each pair of matched diodes, \(D_{21}\) to \(D_{36}\), forms an AND-gate with one of the five input channels.

An input signal of any channel switched to STROB does not produce an output unless a coinciding logic strobe signal is applied. Similarly, a complementary logic strobe signal will not veto in the steady state, but only during the presence of a pulse.

When, for example, the top channel is switched to STROB, \(D_{21}\) conducts \(\sim 4\) mA (while \(D_{22}\) is off), thus reducing the tunnel-diode bias by that amount.
When a logic level is applied to the strobe input, D₁₁ is cut off and D₁₂ conducts the 4 mA. The tunnel-diode bias is restored to 2.7 mA and the logic signals applied to channel 1 input are able to switch the tunnel-diode into its high state.

In the strobed mode, the input impedance of each channel is slightly modified by the presence of D₁ and its bias chain (R₆₁, R₇₁), as this diode is now conducting. The result of this is a slight (~ 5%) improvement in input matching, in the strobed mode over that in the "on" mode.

The emitter-follower T₃ and its associated components provide the necessary current gain and the correct bias for diodes D₁₁ to D₁₈.

3. THE D.C. TRIGGER CIRCUIT AND ITS CONNECTION TO THE DISCRIMINATOR CIRCUIT

A more detailed understanding of the d.c. trigger circuit can be obtained by referring to Fig. 4, in which the tunnel-diode characteristic of D₇, with a number of load-lines, has been drawn. These load-lines are determined by calculating the current absorbed by R₅, the coupling network R₇ and D₉, and the input and strobe circuits as a function of the voltage across the tunnel-diode D₇. The equivalent circuits, which have been used for this calculation, are shown in Fig. 5 (the small difference in the diode currents of Fig. 5a and Fig. 3 is due to there being nothing connected to the input in Fig. 3, whereas a generator having 50 Ω source impedance is connected in Fig. 5a).

P₁ is the steady-state operating point in the on mode or the intermediate operating point when the input and strobe signals do not coincide. P₂ is the steady-state operating point in the strobed mode. All load-lines converge a L₀, which represents the theoretical case where the voltage across D₇ has gone so far positive that all the current in D₄ and D₁₁ has been reduced to zero. The low-state load-line (c) is shown as the addition of the two load-lines (a) (discriminator D₉ and coupling circuit R₇ and D₆) and (b) (R₅, D₅, D₆ and the input circuit).

The low-state load-line (d) for the strobed mode is similar to (c), but having the additional effect of diodes D₁₁, D₁₂, and the strobe buffer circuit added.

When coinciding input and strobe input signals are present, the operating point is H and both load-lines will move to the right (by 800 + 4 × 30 mV = 920 mV) such that the converging point is now L₁.

A high-conductance junction diode (D₉) has been used in the coupling network, in preference to a back-diode, because of its lower junction capacitance. This results in less interaction between the two trigger circuits when D₉ is in the high state, and thus results in an output pulse having a width that is little affected by the overlap time.

4. THE DISCRIMINATOR

The discriminator senses, via the coupling network R₇, D₉, the signal produced by the AND-gate and delivers a signal of well-defined shape to the output circuit. It consists basically of a tunnel-diode monostable circuit with coaxial cable timing [see, for example, van Zurk*].
On receipt of a signal above threshold, \( D_9 \) will switch to the high state, and a negative voltage step will be injected into its load, the coaxial cable \( N_1 \). The voltage will return, with opposite polarity, after twice the propagation delay \( (\tau) \) of the cable, owing to reflection at the shorted end. This reflected signal will reset the tunnel-diode to the low state, and because of this a positive voltage step will now be sent down the cable. After \( 2\tau \) this will return inverted and bring the tunnel-diode back to its original operating point.

Figure 6 shows the tunnel-diode \( (D_9) \) characteristic, composite characteristics, and various load-lines. From these curves the voltages and currents occurring during the steady state and one pulse cycle can be read. \( P_1 \) is the steady-state operating voltage point, defined by the bias current and curve (b). When triggered, the load-line (f) is valid and the high-state \((0 < t < 2\tau)\) operating point will be \( P_2 \), defined by (a) and (f) or (c) and the steady-state bias current. During the reset period \((2\tau < t < 4\tau)\), the operating point is \( P_3 \), defined by (g) and the tunnel-diode characteristic, or by \( I_{P_2} \) and curve (c). If the drive from \( D_7 \) is still present during this time, the voltage will be higher than \( V_{P_3} \), and it is obvious that if this drive lasts longer than \( 4\tau \), a second output pulse will be produced. This places a limit on the overlap time, which should not exceed \( 4\tau \) or \( 17 \mbox{nsec} \) in the present case.

The minimum trigger current is \( \sim 0.7 \mbox{mA} \) (see Fig. 6). The curve (d) indicates the sum of the bias current plus the possible contribution from \( D_7 \) when it is driven high [the method of calculating this curve has been described elsewhere\(^5\)]. There is only one crossing point \((P_2)\) with the composite curve (c), and thus when \( D_7 \) is driven high \( D_9 \) must follow.

5. THE OUTPUT CIRCUIT

The negative signal from the discriminator is buffered by \( T_1 \), then amplified and inverted by \( T_2 \). The voltage gain of this stage is \( \sim 4 \), providing a positive signal of \( \sim 1.6 \mbox{V} \) for the output transistor diode switch\(^6\) \((T_3, D_{13}, T_4)\). Diodes \( D_{16} \) to \( D_{18} \) (and those in identical positions) are to provide output protection and clamping.

6. PERFORMANCE

The performance of the instrument is summarized by the specifications in Fig. 7.

Typical output waveforms are shown in Fig. 8. Figures 9 and 10 illustrate two modes of strobed operation using logic and complementary logic strobe signals which produce an overlap time of \(< 4\tau \). This results in the expected single output pulses when an input pulse coincides with a "I" level strobe signal. In Fig. 11 the overlap is \( > 4\tau \), which results in the second output pulse shown.

The minimum input width (specified \( \leq 1.5 \mbox{nsec} \)) is illustrated in Fig. 12. This is measured in the strobed mode with a d.c. logic level on the strobe input.

The same parameter for the strobe input is shown in Fig. 13 where the d.c. logic level is, in this case, applied to the input.

The maximum repetition rate with the standard timing cable \((N_1 : \tau = 4.25 \mbox{nsec})\) is \( \sim 59 \mbox{MHz} \) and this can be increased with shorter lengths. In Fig. 14, \( N \) was reduced until the limitation in the maximum rate was reached. The input channel was switched to ON, and an input applied of such length as to produce several output pulses. In this case the maximum repetition rate obtained was about \( 170 \mbox{MHz} \) with a cable of \( 30 \mbox{cm} \) \((N_1 = 50 \mbox{cm} = 1.5 \mbox{nsec})\).
The output pulse width varies somewhat when the overlap time is moved through the time $2\tau$ (see Section 3); in all cases this variation is $\leq 700$ psec.

The instrument has been designed to function in an environment having temperatures ranging from $0^\circ$C to $60^\circ$C.

The results of an extensive range of tests on two of these units, randomly selected from production, have been described by Bianchetti and Righini$^7$.

In addition to the applications described, the instrument can be used in many other ways, such as a time digitizer (see Fig. 14), a pulse shaper, etc.
REFERENCES


2) H. Verweij, Proc. Int. Symposium on Nuclear Electronics, Versailles (1968), Tome 1, pp. 60.1 to 60.15.


Fig. 1 Views of unit, shield removed.
Fig. 2 Functional block diagram
Fig. 4  Load-lines on the characteristic of D7.

a) Steady-state loading due to $R_7$, $D_8$ and $D_9$.
b) Steady-state loading due to $R_5$, $D_5$, $D_6$, and input circuit in ON condition.
c) Composite steady-state load-line in ON condition (addition of load-lines a and b).
d) Composite steady-state load-line in STROB condition (addition of load-line c plus loading of $D_{21}$, $D_{22}$, and strobe buffer circuit).
Fig. 5  Equivalent circuits of input and strobe buffer used in the calculation of load-lines.

a) Complete circuit.

b) Simplified circuit.
Fig. 6 Characteristic of D₉ and its load-lines.

a) Tunnel-diode characteristic D₉.
b) Composite characteristic of D₉ and its load in steady state (load R₁₀//R₁₁ = 43 Ω only).
c) Composite characteristic of D₉ and its load under transient conditions (load is R₁₀//R₁₁ = 43 Ω + 50 Ω cable), drawn from steady-state bias current.
d) Bias current plus the possible contribution from B₇ (through D₉).
e) Steady-state load-line (R₁₀//R₁₁ = 43 Ω).
f) Transient load-line (43 Ω + 50 Ω cable, must be drawn through P₁ as indicated).
g) Transient load-line, valid during reset period (2τ < t < 4τ and Tᵢₙ < 2τ).
### INPUT

- **Impedance**: 50 Ω
- **Reflections**: In ON state ≤ 20%  
  In STROB state ≤ 15%
- **Voltage**: Logic -800 mV
- **Width**: Minimal pulse-width to produce output  
  ± 1.5 nsec (at min. "I" level = -600 mV)  
  Maximum, 17 nsec (limited to twice the output width).
- **Maximum rate**: ± 50 MHz determined by output specifications.

### OUTPUT

- **Number**: 1 logic  
  1 complementary
- **Impedance**: High, current source, unused outputs need not be terminated.
- **Width**: 8.5 ± 1 nsec (at -600 mV level for logic  
  and at -200 mV for complementary).
- **Rise- and fall-times**:  
  - Logic:  
    - $T_{RI}$: ≤ 1.6 nsec,  
    - $T_{FI}$: ≤ 2.2 nsec  
  - Complementary:  
    - $T_{RI}$: ≤ 1.6 nsec,  
    - $T_{FI}$: ≤ 1.8 nsec
- **Overshoot**: ± 15%
- **Maximum rate**: ≥ 50 MHz
- **Propagation delay**: 5.5 ± 0.7 nsec

### STROBE

Front panel switch controlled. In position ON outputs are produced on the application of input signals, without the necessity of a strobe signal. In position STROB, inputs will produce outputs only if the logic level (min. ~600 mV d.c. or pulse) is present at the strobe input.

- **Impedance**: 50 Ω
- **Reflections**: ≤ 18%
- **Voltage**: Logic (-800 mV) for strobing on  
  Complementary logic for strobing off.
- **Propagation delay**: Delays of STROB and IN's are equalized  
  up to the input AND-gate.
- **Width**: Minimal pulse width for on and off strobing ≤ 2.0 nsec (at -600 mV for  
  logic and at -200 mV for complementary  
  logic pulses).  
  Maximum: d.c.
- **Rate**: ± 50 MHz, determined by output specifications.

### POWER CONSUMPTION

- 24 V: 240 mA ± 5%  
- -24 V: 400 mA ± 5%

**N.B.**

1. Rise-times ($T_{RI}$) and fall-times ($T_{FI}$) are measured between maximum output "0" (~100 mV) and minimum output "1" (~-900 mV).
2. All parameters have been determined with input signals having rise-times and fall-times of 0.7 nsec.

---

**Fig. 7 Specifications**
Fig. 8  Output waveforms
  a) Logic
  b) Complementary logic

Scale: Hor. 2 msec/div. Vert. 200 mV/div.
Fig. 9  Logic strobed operation, with overlap time < 4τ.
   a) Strobe input
   b) Input
   c) Output

Scale: Hor. 10 nsec/div. Vert. 400 mV/div.

Fig. 10  Complementary logic strobed operation, with overlap time < 4τ.
   a) Strobe input
   b) Input
   c) Output

Scale: Hor. 10 nsec/div. Vert. 400 mV/div.
Fig. 11  Logic strobed operation, with overlap time > 4τ.
   a) Strobe input
   b) Input
   c) Output

Scale: Hor. 5 nsec/div. Vert. 400 mV/div.

Fig. 12  Minimum input width, with d.c. level on strobe input
   a) Input
   b) Output

Scale: Hor. 2 nsec/div. Vert. 400 mV/div.
Fig. 13  Minimum strobe input width, with d.c. level on input
Scale: Hor. 2 nsec/div. Vert. 400 mV/div.

Fig. 14  Maximum repetition rate in ON mode with non-standard timing cable (N₁)
a) Input
b) Output
Scale: Hor. 10 nsec/div. Vert. 400 mV/div.