THE SROD MODULE FOR THE ATLAS TILE CALORIMETER UPGRADE DEMONSTRATOR

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Outline

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- ATLAS Tile Calorimeter
- Phase II Upgrade
- Tile Demonstrator Project
 - ▣ Front-end electronics
 - ▣ Back-end electronics
- sROD demonstrator prototype
- sROD firmware
- Preliminary tests results
- Summary

ATLAS Tile Calorimeter

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- Segmented calorimeter made of steel plates and plastic scintillator which covers the most central region of the ATLAS experiment
 - Divided in 4 partitions: each one has 64 modules
 - One drawer hosts up to 48 Photo Multiplier Tubes (PMTs)
 - The front-end electronics digitize and store the signals coming from PMTs upon the reception of a Level-1 trigger accept, when they are transferred to the Read-Out Drivers (ROD) in the back-end electronics
 - More than 10,000 readout channels

Tile Calorimeter Phase II Upgrade

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- Large Hadron Collider plans to increase the instantaneous luminosity by a factor 7 around 2024 (High Luminosity LHC)
- Complete redesign of front-end (FE) and back-end (BE) electronics
 - ▣ Full **digital** Level-1 trigger
 - ▣ Higher reliability and robustness, higher radiation tolerance
 - Full redundant readout data links
 - Increased modularity in front-end and redundant low voltage power supplies

Current architecture

New architecture

	Present	Phase II
Total BW	~165 Gbps	~40 Tbps (+40 Tbps)
N. fibers	256	4096 (+4096)
BW/drawer	640 Mbps	160 Gbps (+160 Gbps)

13-Nov-14

Tile Demonstrator Project

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- Evaluation and qualification of the new front- and back-end electronics
- Plans for 2015
 - ▣ Test of the complete electronics readout chain during 2015 at CERN using test beams
 - ▣ Possibility of installing a demonstrator drawer into the detector in the shutdown at the end of 2015
- The demonstrator will combine new front- and back-end electronics but still using the present analog trigger system

Front-End Electronics

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- 3-in-1 cards (U. Chicago)
 - Reception and shaping of PMT signals: analog output in two different gains (1, 32)
 - Charge injection calibration capabilities
 - Integrator for physics calibration
 - 17-bit dynamic range with 12-bit resolution

3-in-1 card block diagram

3-in-1 card

- Main Board (U. Chicago)
 - Digitize signals coming from twelve 3-in-1 cards
 - Control of the 3-in-1 cards
 - Low power voltage redundant distribution for all the FE electronics

Main Board

- Daughter Board (Stockholm University)
 - High speed path between front- and end-electronics
 - Control and management of the FE electronics
 - LHC clock distribution
 - Two QSFP optical modules
 - Two Kintex 7 FPGAs

Daughter Board version 3

Mechanics – Mini-Drawers

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- Super-drawer demonstrator will be composed of 4 mini-drawers, each one containing
 - ▣ 1 adder base board + 3 adder cards
 - Analog data to the present L1Calo system
 - ▣ 12 x 3-in-1 card1 + 12 x PMT
 - ▣ 1 Main Board
 - ▣ 1 Daughter Board
 - ▣ 1 HV regulation board

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Back-End Electronics

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□ Super Read-Out Driver (sROD) demonstrator (IFIC-Valencia)

High speed interface with the front-end electronics

- BW: 4 x 40 Gbps
- Readout data coming from the detector
 - 4 Mini-Drawers
 - Up to 48 PMTs
 - Timing Trigger and Control (TTC) distribution to the FE
 - Clock distribution for synchronization
 - Control and configuration commands
 - Real time data processing
 - Reconstruction algorithms: energy, time and quality factor
 - Communication with the Level-1 Trigger system
 - Sending preprocessed data for L1 trigger decision
 - Keeps backward compatibility with the present DAQ system

Schema of the sROD demonstrator

sROD prototype

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Xilinx Spartan 6

- Slow control capabilities (Clock management)
- Read back status of the system (IPMI port)

Module Management Controller (MMC)

- Power connection management
- IPMI protocol

2 x CDR IC

- ADN2814
- Clock/data from TTC

DDR3 512MB

Xilinx Kintex 7 FPGA

- XC7K420T
- 28 GTX transceiver @ 10 Gbps
- Data preprocessing
- Communication with Level 1 trigger system

Xilinx Virtex 7 FPGA

- XC7VX485T
- 48 GTX transceiver @ 10 Gbps
- Communication with FE electronics
- Data processing

AMC connector

- 12 V power connection
- Slow control path
- High-speed communication path with the carrier board / μ TCA crate (GbE, PCIe, custom protocols)

FMC connector

- Expansion functionalities: ADC boards, test boards, ...

DDR3 512MB

sROD prototype

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Power Modules

- Linear Technologies
- Low noise

Jitter cleaners

- TI CDCE62005
- Low jitter (< 1ps)
- Clean recovery clocks for GTX
- Unify clock domains

Power supervisory IC

- LT LTC2977
- Power sequencing
- Protection
- Current, voltage, temp.

MiniPOD TX

- 12 x 10 Gbps
- L1 trigger communication

UART-USB ports

Ethernet port

- 10/100/1000 Mbps
- PC communication

SFP module

- TTC reception
- Communication with current DAQ system

4 x QSFP modules

- FE communication
- Each module at 40 Gbps
- Total max. BW: 160 Gbps

MiniPOD RX

- 12 x 10 Gbps
- Test purposes

Clock generator

- LMK03806B
- 10 diff outputs
- Low jitter

JTAG programmer

sROD prototype- Design

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- Stack-up
 - Dielectric Nelco N4000-13
 - 16 layers ~ 1.6 mm
 - 8 for power/ground planes
 - 8 for signals
- 3D Electromagnetic field simulations
 - Minimization of impedance discontinuities
 - Differential vias in Gbps lines
 - Return/signal via geometry
 - DC block capacitor
 - Small hole under package
 - Trace geometries
 - Single micro/striplines
 - Differential micro/striplines
- Noise studies in analog power planes
 - Strong requirements
 - Maximum voltage ripple for GTX analog power planes tolerate is 10mVpp

ATCA platform test-bench

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- ❑ Adopted by ATLAS as VME replacement
- ❑ Double mid-size AMC form factor
 - 180.6 mm x 148.5 mm
 - μ TCA crates/ATCA carrier boards + ATCA crate
- ❑ Complete ATCA test-bench from Radisys
 - SYS6006 chassis
 - ATCA 4500 CPU
 - ATCA-1200 carrier
 - A1200 Rear Transition Module
- ❑ ELMA 6U slot chassis
 - Pigeon Point Shelf Manager
- ❑ DCS integration with ATCA: fwATCA 1.0 application
 - Integration with the DCS server (WinCC) through SNMP
 - Control and monitor the chassis

Name	Value	Thresh	Type	OID
setPowered	1	-	INT	1.3.6.1
ipmbAddress	136	-	INT	1.3.6.1
present	1	-	INT	1.3.6.1
getPowered	1	-	INT	1.3.6.1
manufacturer	Radisys Corp.	-	STRING	1.3.6.1
healthy	1	-	INT	1.3.6.1
slot	4	-	INT	1.3.6.1
reset	0	-	INT	1.3.6.1
name	ATCA-1200	-	STRING	1.3.6.1

Standard data points

fwATCA 1.0

sROD demo

ATCA carrier

ATCA crate

sROD Firmware

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- sROD emulator: Xilinx VC707 Evaluation Board for tests

- Implementation of high-speed protocols

- GigaBit Transceiver (GBT) protocol developed at CERN

- sROD requires of an asymmetric bandwidth:

- 4 x 4.8 Gbps for downstream per mini-drawer
 - 4 x 10.24 GBps for upstream per mini-drawer

4 x 10.24 Gbps
4 x 4.8 Gbps

- Data processing and management

- Readout data received every Bunch Crossing

- Stored in pipeline memories

- TTC decoding and transmission

- FE electronics configuration and read-back
 - Test and calibration applications

- DCS command un/packing

- DCS configuration and read-back

- Communication with present DAQ

- TTC reception

- G-Link emulator (to current ROD)

- Interface communications

- Ethernet port + Ipbuss protocol

Firmware block diagram

Daughter Board

Main Board

3-in-1 card

Valencia test-bench

PC

sROD emulator

Complete sROD schema

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Preliminary test results

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- Complete test-bench with PMT blocks, new front- and back end electronics and mechanics
- There is a lot of progress during the last months:
 - ▣ Front-end control and configuration
 - sROD (VC707) + PC
 - ▣ Readout of calibration data from PMTs
 - Charge injection pulses and integrator data
 - ▣ Charge injection, pedestal and integrator linearity tests
 - ▣ Read back configuration from front-end
 - 3in1 cards status
 - HV board status
 - ▣ Measured electronic noise on channels

Demonstrator test-bench at CERN

CH2: integrator linearity test

CH2: pedestal linearity test

Assembly of the front-end electronics

Summary

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- R&D projects for Tile Calorimeter Phase II Upgrade are progressing
 - ▣ Complete redesign of the front-end and back-end electronics for Phase II Upgrade
- sROD demonstrator
 - ▣ First hardware prototypes have been produced
 - ▣ Firmware developments based on Xilinx VC707
- Tile Demonstrator Project
 - ▣ First versions of the new front-end electronics are available
 - ▣ Early tests are showing promising results
 - ▣ Test of electronics using test beams during 2015
 - ▣ Possibility of insert the new electronics in the shutdown at the end of 2015

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BACK-UP SLIDES

Firmware – sROD Emulator

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- Xilinx Evaluation board VC709
 - ▣ +SFP+/QSFP+ FMC Module (HiTech)
- Firmware development ongoing
 - ▣ Upstream/Downstream communication with 1/4 Mini-drawer
 - DCS
 - Readout
 - ▣ Firmware will be migrated to sROD demonstrator
 - ▣ First PROMETEO (Portable ReadOut Module for Tilecal ElectrOnics) prototype
 - Natural replacement of MobiDICK 4 test-bench
 - Future versions will be based on sROD demonstrator

sROD Firmware

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- Xilinx Evaluation board VC707
 - ▣ Commercial FMC card with two slots for QSFP modules (40 Gbps each)
 - ▣ Dedicated FMC card for receiving TTC signals (CERN)
 - ▣ Communication with PC via Ethernet

Xilinx VC707 Development Kit

PC

sROD emulator

Main Board

3-in-1 card

Valencia test-bench

Software - TilelpmiGui

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- Complete ATCA test-bench in bld. 175
- TilelpmiGui monitors the ATCA modules through IPMI bus
 - ▣ TileIPMI library makes use of the open source OpenIPMI library
- Provides connection to the Shelf Manager through the fabric interface using the CPM
 - ▣ Using the name of the IPMI Server from any machine at CERN
 - ▣ Version 0: Shows the information of the main boards and FRU detected in the ATCA shelf
 - GLIB AMC (CERN)
- Next steps: include different panels to read and monitor the sensors of the ATCA boards

TilelpmiGui – Qt

TileIPMI – C++

OpenIPMI

Firmware – sROD Emulator

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□ Diagram