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A digital readout system for the CMS Phase I Pixel Upgrade

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Abstract

The Phase I Upgrade to the CMS Pixel Detector at the LHC features a new 400 Mb/s digital readout system. This new system utilizes upgraded custom ASICs, PSI46dig Read Out Chips (ROC) and Token Bit Manager (TBM08/09) for data packaging, new optical links, and changes to the Front End Drivers (FEDs). We will be presenting the new architecture of the full readout chain, the new schema for data encoding/transmission, and the results of preliminary testing of the new components.

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A Digital Readout System for the CMS Phase I Pixel Upgrade

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ABSTRACT: The Phase I Upgrade to the CMS Pixel Detector at the LHC features a new 400 Mb/s digital readout system. This new system utilizes upgraded custom ASICs, PSI46digv2.1 Read Out Chips and Token Bit Manager for data packaging, new optical links and changes to the Front End Drivers. We will be presenting the new architecture of the full readout chain, the new schema for data encoding/transmission, and the results of preliminary testing of the new components.

KEYWORDS: CMS; Phase I; Pixel.

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1. CMS Phase I Pixel Detector

The CMS Phase I Pixel Upgrade [1] will replace the current CMS Pixel Detector in the CMS Detector at the LHC in 2017. The upgraded detector has four barrel layers and three forward disks, compared with three and two in the current detector. The detector will have twice the number of modules that must be read out using the same optical fiber infrastructure without adding new fibers. Reusing the original fibers puts a further limitation that both the sender and receiver must be compatible with the existing 1310nm fibers [2]. A comparison of the current and upgraded detector is shown in Figure 1.

The current CMS Pixel Detector uses a 40 MHz digitally encoded analog signal. Different analog levels express header, trailer, and other markers in the data stream. However, 40 MHz is not optimal for the new optical receivers to be used by the Phase I Pixel. The modules for the upgraded detector have 16 new digital readout chips (ROCs), PSI46digv2.1, which operate at 160 Mb/s [3], replacing the 40 MHz analog ROCs. The Token Bit Manager (TBM) chip used in the upgrade modules, TBM08b, is an upgrade from the TBM05 [4] that is used in the current CMS Pixel analog modules. The new TBM chip interleaves signals from two streams of 8 ROCs each into a 320 Mb/s stream and then encodes the data into a 400 Mb/s stream that is sent from the module. Each of the 16 ROCs in a Pixel Detector module is bonded to a silicon sensor with 4160 individual pixels. Each module has one TBM to manage the readout. The TBM has dual processing cores that read out eight ROCs each as shown in Figure 2.

a) The present detector is shown on the left with the Phase I detector on the right.

b) The present detector is shown on the bottom and the Phase I detector is on the top.

Figure 1. A comparison of the current CMS pixel detector and the Phase I upgrade.

Figure 2. The elements of the TBM08 chip.

2. CMS Phase I Pixel Readout Chain

After encoding, each module outputs a single differential signal. These electronic signals must be converted to optical for transmission. For the FPIX, the electronic signals travel to a “port card” located in the detector while the BPIX uses a similar “POH-motherboard”. Both boards contain a pixel optohybrid (POH) [5], which uses a digital level translator (DLT) and an optical driver to produce the optical output. The signals travel from the detector on optical fibers to the front end drivers (FED) several hundred meters from the detector. The FEDs are responsible for decoding the module data and constructing events to be sent to the data acquisition system.

The prototype Phase I Pixel FEDs are upgraded Pixel FEDs with the deserializer FPGAs replaced by an additional daughter card for decoding the digital signal. The daughter cards have optical receivers that operate most efficiently at higher speeds. There are two types of optical receivers being used for the Phase I Pixel FEDs, the Zarlink and the Fitel. The Zarlink receiver is used in the prototype Pixel FEDs, while the Fitel will be used in the next generation of Pixel FEDs. The choice of 400 Mb/s as well as the encoding is to provide the receivers an appropriate signal speed and provide approximately equal numbers of 0's and 1's to help minimize errors. The Pixel FED contains custom firmware for decoding and parsing the incoming pixel data.

When a trigger is received, a new event begins. The start of an event is indicated by the presence of a TBM header and the end by a TBM trailer. Between the header and trailer, ROC headers and pixel data are inserted. Following each TBM header and trailer is 16 bits of status information including event number and error flags. The ROC headers are used to separate the pixel hits to identify the chip where the hit occurred. Each pixel hit is encoded within 24 bits to contain the position of the hit and the pulse height ADC.

Between events, the ROCs are in the idle state. When ROCs are idle, 1s are continually sent. After encoding, the continuous 1 state becomes a repeating “idle” pattern of 12.5 ns high then 12.5 ns low, which represents a binary pattern of 11111 and 00000 (Fig. 3).

a) 40 MHz Analog Signal

b) 400 Mb/s Digital Signal

Figure 3. a) The 40 MHz digitally encoded analog signal with the different address levels. b) The 400 Mb/s digital signal including idle pattern and event.

2.1 Encoded data format

To create a single output stream from the two TBM cores and provide a signal format that is robust and optimized for the optical receivers, the data is encoded for transmission. To encode the data, the TBM multiplexes the two data streams and then encodes them using a 4 to 5 bit scheme and Non Return to Zero Inverted (NRZI) [6] encoding to reduce errors in the optical transmission.

When the data streams from the two TBM cores are multiplexed, the second stream is inverted. Every four bits of the multiplexed data stream is then defined as a “word” that is translated into a 5-bit equivalent via a lookup table. The 4 to 5 bit encoding maps the 16 values of the 4-bit address space onto the 32 possible values of the 5-bit address space. By leaving half of the possible values unused, we introduce the possibility to identify transmission/decoding errors. If the decoded 5-bit word does not correspond to a used value then it is clear there was an error.

Non-Return to Zero Inverted encoding is a well-established standard for data encoding for transmission. The NRZI format seeks to produce an equal number of 0s and 1s in the digital signal by maximizing the number of high/low transitions. In an NRZI encoded signal, if the value to be sent is a 1 then the complement of the previous bit is sent, if a 0 is to be sent then the previous bit is repeated. Since NRZI output is dependent on the previous bit, each 5-bit word will have two possible values, one for a previous bit of 0 and one for a 1. These two values will be complements of each other.

Since the data is organized into 5-bit words, it is critical to correctly identify the start of each word. Each word can be interpreted differently depending on the choice of starting position (Fig. 4). To be able to identify the start of each 5-bit word uniquely, a special “framing” pattern is introduced. The 5-bit patterns 11011 and 00100, which represent the same value because of the NRZI encoding, are replaced by 11111 and 00000, respectively. These values cannot appear anywhere in the datastream and therefore can be used to uniquely define the start of the word.

Figure 4. Every nine bits contain five different interpretations of the 5-bit word, only one is correct.

Each time the framing pattern is received, the serial decoder is realigned to the start of the 5-bit word. The framing pattern replacement is done every time the 11011 or 00100 pattern is sent, which is continuously if the ROCs are idle as these values are the encoded idle pattern, or occasionally in the event packets.

3. Full Chain Tests

Tests of the full readout chain have been performed to determine the error rate and verify that it is within acceptable limits. Prior to the production of prototype components, preliminary tests involved a simulated data stream produced by a custom FPGA testboard with module emulation firmware. The testboard was connected directly to a prototype POH for conversion to an optical signal. The optical signal was decoded by the same prototype Pixel FED with Zarlink receiver as will be used in the first tests of the upgrade. Over 500k simulated events were decoded without error representing a bit error rate $< 10^{-8}$.

Figure 5. A Bit Error Rate tester was used with optical attenuation to extrapolate the error rate.

Error rates are required to be less than 10^{-12} and expected to be less than 10^{-15} . Measuring the error rate directly at 400 Mb/s would not be practical; at 10^{-15} one error would occur every 11.6 hours. To measure the rate faster, the signal is attenuated and the error rate is extrapolated. To measure the error rate after attenuation a Bit Error Rate Tester (Fig. 5) was used with a POH and a Fitel optical receiver, which will be used in the next generation of Pixel FEDs. The POH tested had seven laser drivers (LD1-7). The error rate was plotted vs. the optical module amplitude (OMA) at the receiver. At the expected signal levels, the extrapolated error rate was shown to be less than 10^{-12} .

4. Summary

The CMS Phase I Pixel Upgrade's new digital readout system was designed to be robust at 400 Mb/s, while still being compatible with the existing CMS infrastructure. The data encoding scheme introduces error checking and signal optimization for transmission. Tests of the full chain, from module to FED, as well as bit error rate tests of the optical links show acceptably low error rates for the system.

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