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Near Future Upgrades for the CMS Pixel Detector

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Abstract

The silicon pixel detector is the innermost component of the CMS tracking system, providing high precision space point measurements of charged particle trajectories. The current pixel detector is designed to operate at a maximum luminosity of $1 \times 10^{34} \text{cm}^{-2} \text{s}^{-1}$. Before 2018 the instantaneous luminosity of the LHC is expected to reach $2 \times 10^{34} \text{cm}^{-2} \text{s}^{-1}$, which will significantly increase the number of interactions per bunch crossing. The performance of the current pixel detector in such high occupancy environment will be degraded due to substantial data-loss and effects of radiation damage of sensors, built up over the operational period. In order to maintain or exceed its current performance, the CMS pixel detector will be replaced by a new lightweight system with additional detection layers, better acceptance and improved readout electronics. The upgraded pixel detector will provide improved track and vertex reconstruction, standalone tracking capabilities, as well as identification of particles with longer lifetimes, which will be crucial elements of many physics analyses.

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Near Future Upgrades of the CMS Pixel Detector

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ABSTRACT: The silicon pixel detector is the innermost component of the CMS tracking system, providing high precision space point measurements of charged particle trajectories. The current pixel detector is designed to operate at a maximum luminosity of $1 \times 10^{34} \text{cm}^{-2} \text{s}^{-1}$. Before 2018 the instantaneous luminosity of the LHC is expected to reach $2 \times 10^{34} \text{cm}^{-2} \text{s}^{-1}$, which will significantly increase the number of interactions per bunch crossing. The performance of the current pixel detector in such high occupancy environment will be degraded due to substantial data-loss and effects of radiation damage of sensors, built up over the operational period. In order to maintain or exceed its current performance, the CMS pixel detector will be replaced by a new lightweight system with additional detection layers, better acceptance and improved readout electronics. The upgraded pixel detector will provide improved track and vertex reconstruction, standalone tracking capabilities, as well as identification of particles with longer lifetimes, which will be crucial elements of many physics analyses.

KEYWORDS: Particle tracking detectors; Performance of High Energy Physics detectors; Solid-state detectors.

*On behalf of the CMS Collaboration

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1. The CMS pixel detector

The Compact Muon Solenoid (CMS) experiment [1] at the CERN Large Hadron Collider (LHC) has the largest ever built all-silicon tracking system with a pixel detector as the innermost component. The pixel detector [2], enclosed in a superconducting solenoid producing a 3.8 T magnetic field, comprises of three 53 cm long cylindrical barrel layers (BPIX) at radii of 4.4, 7.3 and 10.2 cm from the interaction region, complemented with two disks (FPIX) on each end at $z = \pm 34.5$ cm and $z = \pm 46.5$ cm extending from 6 to 15 cm in radius. The pixel detector covers a pseudorapidity range up to $|\eta| = 2.5$, matching the acceptance of the central tracker. There are approximately 66 million pixels in the system with a cell size of $100 \mu\text{m} \times 150 \mu\text{m}$. Due to its excellent spatial resolution, the pixel detector has the key role to provide the precise spatial measurements used as seeds for the reconstruction of charged particle trajectories in the proximity of the primary interaction point. Its performance is thus crucial for the identification of primary and secondary vertices, quantities that are essential for the efficient identification of long-lived particles, such as b quarks, and for the search of new physics at the LHC.

2. Motivation for the upgrade

The current detector was designed to operate at a peak instantaneous luminosity of $1 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ and has performed very well during the first run of the LHC (2010-2012). The pixel detector has operated at high efficiency, with 96% of its channels functional, with a high hit efficiency of 99%, and good spatial resolution ($9 \mu\text{m}$ in $r - \phi$ and $20 \mu\text{m}$ in z). During the coming years, however, the performance of the LHC will be improved in steps, and a instantaneous luminosity of around $2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ is anticipated before 2018. Depending on the bunch spacing, the number of overlapping interactions per bunch crossing (referred to as pileup) will increase to 50 (25 ns bunch crossing time) or 100 (50 ns bunch crossing time). This leads to an increase in the track density and hit rates, with hit rates of up to 600 MHz cm^{-2} in the worst case in the innermost barrel layer. Under such conditions, the inefficiency in the readout chip would increase dramatically, from its current value of up to 4% to up to 16%, or even 50%, for bunch crossing intervals of 25 and 50 ns, respectively. The tracking performance of the pixel detector will also be significantly degraded due to effects of radiation damage built up over several years of operation. The Phase-1 upgrade to the pixel detector is planned to accommodate these running conditions [3].

3. Elements of the upgrade

The Phase-1 pixel detector will need to survive 500 fb^{-1} of integrated luminosity and maintain high efficiencies and low fake rates at the expected 50 or more pileup events. The Phase-1 pixel detector will seek to reduce material and minimize degradation due to radiation damage. Data loss will be minimized with an improved and faster readout system. The upgraded pixel detector is scheduled to be installed inside CMS during the technical stop of 2016/2017. The upgraded pixel system is constrained by the existing insertion volume and services, which will remain unchanged during Phase 1. Therefore, it must re-use as much as possible the existing services (cables, pipes, optical fibers, etc.).

3.1 Additional detection layers

Figure 1 shows overview of the new detector design. Key features are an additional fourth barrel layer at 16.0 cm radius and one additional end cap disk on either side at $z = \pm 51.4 \text{ cm}$, providing 4 pixel-hit coverage over the full acceptance ($|\eta| < 2.5$). The innermost layer is moved closer to the interaction point (radius reduced from 4.4 cm to 2.9 cm) which is possible due to new smaller diameter beam pipe; this will improve the track impact parameter resolution. The forth layer is added closer to the Tracker Inner Barrel (TIB); this will significantly improve the pattern recognition in the high occupancy environment, providing at the same time a safety factor in case the first silicon strip layer degrades more rapidly than expected.

The number of modules (pixels) for BPIX increases from 768 (48 million) to 1184 (79 million). The modules will be mounted on carbon fiber ladders glued onto stainless steel cooling tubes. FPIX uses the same module design as BPIX. The total number of FPIX modules stays constant at 672, while the number of pixels increases from 18 to 45 millions. The FPIX support structure will be made of blades arranged radially into half-disks, with a similar turbine like geometry as in the present detector. Each half-disk will be composed of two concentric rings, to remove and replace

Figure 1. The layout of the current and Phase 1 upgrade pixel detector (top). The geometry of the upgraded BPIX and FPIX detectors (bottom).

independently the innermost part after radiation damage. Each module on the outer ring is rotated by 20° in a turbine geometry. In order to obtain excellent resolution in both the azimuthal and radial directions throughout the inner ring, the modules are arranged in an inverted cone array with the modules tilted by 12° with respect to the interaction point, combined with the 20° rotation.

3.2 Sensor and readout chips

The silicon sensors use the same n^+ -in-n design of the present detector with $100\ \mu\text{m} \times 150\ \mu\text{m}$ pixel size and a sensor thickness of $285\ \mu\text{m}$. This design has proved to be highly radiation-tolerant because of its ability to operate partially-depleted. Studies with irradiation tests show that the sensor is capable of delivering enough signal for a bias voltage of below 600 V, even after receiving fluences of $1.5 \times 10^{15}\ \text{N}_{eq}\ \text{cm}^{-2}$, corresponding to $250\ \text{fb}^{-1}$ for the innermost layer at a radius of 3 cm.

The basic architecture of the readout chip (ROC) also remains the same; $52\ \text{columns} \times 80\ \text{rows}$ of pixels are bump-bonded to the sensor. The readout is organized in double columns, which operate independently. Zero suppressed hit information for pixels of two adjacent columns is stored in the same buffer at the periphery of the ROC. From there, hits corresponding to events verified by the CMS Level-1 trigger are read-out upon an external token passage. The main data loss of the present pixel detector at high luminosity conditions will be due to limited buffering, speed limitation in the transfer of hits from the pixels to the periphery and dead time of a double column while waiting for the read-out token. Major improvements for the current ROC design have therefore been developed [4].

Figure 2. The amount of material in the pixel detector shown in units of radiation length as a function of pseudorapidity.

The new ROC runs internally with a 160 MHz clock instead of 40 MHz. The output format changes from a multilevel encoded analog signal to a new digital read-out with a 160 Mbits LVDS data link. The digital readout removes the need for the complex decoding of a multilevel analog signal of the current ROC. Major data loss due to overflow of buffers will be avoided by increased time stamp (from 12 to 24) and data (from 32 to 80) buffers in the peripheries. In addition, a new read-out buffer on the ROC has been added to buffer pixel hits, that were verified by the CMS trigger, until the external read-out token passage. The new ROC design with an additional layout layer and a thicker top layer provides reduced internal crosstalk and a lower charge threshold (from 3500 down to 1800 electrons). As a result, for $2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ and 25 ns operation, data loss due to dead time can be kept below 4.7% on the innermost layer, while for the current detector it would amount to about 16%.

3.3 Reduction in material budget

The services (including cables, cooling pipes, and on and off-detector electronics) and the mechanical support structure of the current pixel detector introduce a non-negligible amount of material in the tracking volume, thus reducing the track reconstruction efficiency and degrading the impact parameter resolution. Since the extra pixel layer adds about 50% to the total number of modules, it could easily increase the total amount of material of the pixel detector. To avoid this, the support and services of the upgraded detector have been redesigned to be lighter than in the present system, using ultra-lightweight support with CO_2 cooling, and by relocating much of the passive material, like the electronic boards and connectors, out of the tracking volume. Figure 2 illustrates the material reduction in the pixel detector volume in units of radiation length as a function of η . Particularly in the forward section and the barrel to forward pixels transition region (around $\eta=1.5$), the amount of passive material will be significantly lower. Such a reduction will have a large impact on the charged particle tracking efficiency as well as electron and photon identification and resolution through the reduced rate of secondary interactions of particle with matter.

3.4 New cooling system

Present pixel detector uses a mono-phase C_6F_{14} cooling scheme which is a major source of material budget in the tracking volume. The upgraded detector will use a low-mass two-phase CO_2 cooling system, which could allow for lower operating temperatures, which are beneficial for sensor performance and lifetime. With CO_2 , the system can be operated with thin pipes and in addition a small mass flow provides a high cooling power. As a result the new cooling system provides significant reduction in the amount of material.

3.5 DC-DC powering scheme

The new pixel detector with 123 million pixels will have almost twice the number of electronic channels with respect to the present system. Since front-end power consumption and supply voltages will not change, this translates directly into an increase in the supply current by the same factor. Consequently, power losses on the 50 m long supply cables that link the detector with the power supplies will increase by a factor of almost four. The required total power can not be delivered by the present power supplies, and the heat load on the cables would probably also surpass the tolerable limit. Since a significant addition of more cables is technically excluded and the installation and commissioning of new power supplies is not feasible within a winter technical stop, the pixel detector will feature a DC-DC conversion powering scheme [5]. Step-down DC-DC converters allow the power to be delivered at a higher voltage, but with lower current. Losses on the supply cables are thus reduced by a factor of about ten. These DC-DC converters are installed on the pixel service structures, approximately 1 m away from the modules and outside the sensitive tracking volume.

4. Expected Performance from the upgraded detector

With the expected improvements in the tracking efficiency, track impact parameter resolution, and primary vertex resolutions, the b -tagging performance of the Phase I upgrade pixel detector is expected to be significantly better than the current pixel detector at high pileup. The performance of the CMS "Combined Secondary Vertex" b -tagging algorithm has been studied using a sample of simulated $t\bar{t}$ events. Figure 3 shows the b -tagging efficiencies for the current and upgrade detector in the high luminosity environment of $2 \times 10^{34} cm^{-2}s^{-1}$ for different pileup scenarios and misidentification rates from c -jets and light jets. It can be seen that the b -tagging performance for the upgrade detector is superior to the current detector running under high occupancy conditions of the upgraded LHC with large number of overlapping interactions in each bunch crossing.

5. Pixel modules

One module type will be used in both the barrel and endcap regions. A pixel module contains 2×8 ROCs bump-bonded to a silicon sensor. Wirebond pads on the ROC peripheries extend 2 mm beyond the sensor, along the two long sides of the module. A high density interconnect (HDI) is glued on top of the sensor with wire-bond pads to connect to the corresponding pads on the ROCs. Glued and wirebonded on top of the HDI is the token bit manager chip (TBM). The TBM

Figure 3. The b-tagging performance of the upgraded detector compared to the current pixel detector running at high luminosities of LHC Phase-1. The b-tagging efficiency as a function of range of pileup events for different levels of misidentification rates of light jets (a) and charm jets (b).

Figure 4. Components of the BPIX module (left). Assembled BPIX and FPIX modules (right).

controls the readout of ROCs and distributes clock, trigger, and reset signals and is the interface for directing the downloading of ROC operating constants. Power and signals to the HDI are distributed by an external flex cable. The BPIX and FPIX modules are also equipped with base-strips and end holders, respectively, which permit mounting of the modules on the mechanical structure. Figure 4 shows an assembled BPIX and FPIX module. Eight modules (assembled with prototype components) have been installed into the present FPIX system during LS1 and will be operated during 2015-2016. This "pilot detector" will use existing power, cooling and readout cables from the present system. Operational experience under LHC realistic conditions will be valuable for commissioning the full pixel detector.

6. Summary

The Phase-1 upgrade of the CMS pixel detector is motivated by excellent performance of the LHC as well as accumulated radiation damage. The upgraded pixel detector will be installed in CMS during the extended winter technical stop of 2016/17. Among the new features of the upgraded detector design are extended instrumentation with improved acceptance and precision, significantly

less passive material, new front-end electronics with higher efficiency, and new cooling and powering systems. Simulation studies for the new detector reveal a significantly improved tracking performance compared to the current detector for the luminosities expected for LHC Phase-1. A few pixel modules, the pilot detector, have been inserted into the CMS FPIX system in 2014 to gain operational experience and commission the data acquisition system.

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