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The pixel detector for the CMS phase-II upgrade

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Abstract

The high luminosity phase of the Large Hadron Collider (HL-LHC) requires a major pixel detector R&D effort to develop both readout chip and sensor that are capable to withstand unprecedented extremely high radiation. The target integrated luminosity of 3000 fb^{-1} , that the HL-LHC is expected to deliver over about 10 years of operation, translates into a hadron fluence of $2 \times 10^{16} \text{ 1MeV eq.n. / cm}^2$, or equivalently 10 MGy of radiation dose in silicon, at about 3 cm from the interaction region where the first layer of the pixel detector could be located. The CMS collaboration has undertaken two baseline sensor R&D programs on thin n-on-p planar and 3D silicon sensor technologies. Together with the ATLAS collaboration it has also been established a common R&D effort for the development of the readout chip in the 65 nm CMOS technology. Status, progresses, and prospects of the CMS R&D effort are presented and discussed in this article.

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The pixel detector for the CMS phase-II upgrade

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ABSTRACT: The high luminosity phase of the Large Hadron Collider (HL-LHC) requires a major pixel detector R&D effort to develop both readout chip and sensor that are capable to withstand unprecedented extremely high radiation. The target integrated luminosity of 3000 fb^{-1} , that the HL-LHC is expected to deliver over about 10 years of operation, translates into a hadron fluence of $2 \times 10^{16} \text{ 1MeV eq.n. / cm}^2$, or equivalently 10 MGy of radiation dose in silicon, at about 3 cm from the interaction region where the first layer of the pixel detector could be located. The CMS collaboration has undertaken two baseline sensor R&D programs on thin n-on-p planar and 3D silicon sensor technologies. Together with the ATLAS collaboration it has also been established a common R&D effort for the development of the readout chip in the 65 nm CMOS technology. Status, progresses, and prospects of the CMS R&D effort are presented and discussed in this article.

KEYWORDS: CMS; Upgrade; Pixel.

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1. CMS pixel phase-II upgrade motivations

The major achievement of LHC experiments during 2012 was the discovery of the Higgs particle [1]. Though it is one of the greatest discoveries of the past decades, there are still questions that need to be answered. The entire Higgs sector still needs to be investigated by measuring: the Higgs couplings and properties; the Higgs self coupling; Vector Boson Scattering (VBS) for which are crucial the forward tagging jets. Moreover Standard Model (SM) measurements should be performed such as precision measurements, e.g. W-boson mass, Weinberg angle ($\sin(\theta_W)$), fine structure constant (α_s); search for rare SM processes, enhanced by physics beyond SM (e.g. $B_{s,d} \rightarrow \mu\mu$); differential cross-section measurements of W, Z, di-boson, Top.

All these measurements require to collect a huge amount of data. To this extent an LHC luminosity upgrade is planned by the end of 2021 (HL-LHC). To cope with the LHC upgrade and to improve the measurement reach [2], the LHC experiments are being redesigned (referred to as phase-II upgrade). This article will focus in particular on the pixel detector upgrade of the Compact Muon Solenoid (CMS) experiment [3].

2. Detector operating conditions

The high luminosity upgrade of the LHC (HL-LHC) consists of an upgrade of the damaged low- β triplets (quadrupole magnets next to the interaction point) and the installation of crab-cavities to optimize the bunch overlap. The final beam characteristics should be: energy = 14 TeV; instantaneous luminosity = $5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ (corresponding to ~ 10 times the current instantaneous luminosity); yearly integrated luminosity = $\sim 300 \text{ fb}^{-1}/\text{year}$ (corresponding to a total integrated luminosity in 10 years of 3000 fb^{-1}); 25 ns bunch spacing; average pileup = 140 (to be compared to the current 25); radiation fluence at 30 mm from the interaction point = $2 \times 10^{16} \text{ 1MeV eq.n. / cm}^2$ (corresponding to ~ 10 times the foreseen radiation damage accumulated after the phase-I upgrade [4]); radiation dose at 30 mm from the interaction point = 10 MGy (i.e. 1 Grad); hit rate = $\sim 2 \text{ GHz/cm}^2$ (corresponding to ~ 10 -20 times the current hit rate).

Figure 1. Foreseen LHC upgrade schedule. Both phase-I and phase-II are highlighted.

Figure 1 shows the foreseen LHC upgrade schedule. The phase-II upgrade, which is the subject of the current article, requires a huge R&D from the experiments to cope with such an harsh environment. Indeed the detector designed for the phase-I upgrade, after 500 fb^{-1} of data collected, would experience an impact parameter degradation of more than 50%, and an average pileup of 140 would imply an irreducible data loss of $\sim 7\%$.

The detector degradation would inevitably impact on the physics performance: the efficiency loss would diminish the effectiveness of high- p_T lepton isolation, and would degrade the jet energy and missing transverse energy resolutions, while fake tracks would cause biases and resolution degradation in jet energy measurements, would increase the background levels, and would adversely affect high- p_T lepton isolation criteria.

3. Detector layout choices

The pixel detector layout for the phase-II upgrade will feature an improvement in the resolution of high- p_T tracks and in the two-track separation. This will be achieved by increasing the granularity (indeed the present tracker has degraded track finding performance in high-energy jets due to hit merging in the pixel detector). It is also foreseen a resolution improvement of low- p_T tracks and a reduction of secondary interactions, achieved by reducing the amount of material. Finally an increase of the forward acceptance is also planned to mitigate the pileup effects in jet identification and energy measurement, in order to cover the peak production region of jets from Vector Boson Fusion and Vector Boson Scattering, which are among the highest priorities of the CMS physics

program. To this extent a four layers barrel (the current detector has 3 layers) and ten-plus-ten forward disks (the current detector has two-plus-two) are foreseen as sketched in Fig. 2, covering an overall active area of $\sim 4 \text{ m}^2$, corresponding to ~ 1.5 times the phase-I pixel detector. This design allows for a pseudo-rapidity coverage up to $|\eta| \approx 4$, while the current detector covers up to $|\eta| \approx 2.4$, all in all by preserving the ease-of-access of the current detector which allows for the possibility to replace degraded parts over technical stops.

Figure 2. Foreseen pixel detector layout for the phase-II upgrade.

3.1 Pixel cell size

The readout chip is foreseen to be made in the 65 nm CMOS technology. To test its radiation resistance and to design the fundamental blocks an ATLAS-CMS cross collaboration, called RD-53, has been established (experiment specific design choices will eventually be implemented). The chip cell size should be either $50 \times 50 \mu\text{m}^2$ or $25 \times 100 \mu\text{m}^2$ and the aim is for a relatively large chip of $\sim 20 \times 20 \text{ mm}^2$. The sensor cell for the size $25 \times 100 \mu\text{m}^2$ presents significantly more difficulties in terms of isolation, moreover the minimum pitch for the Indium bump bonding (BB) is $25 \times 100 \mu\text{m}^2$ or $50 \times 50 \mu\text{m}^2$, but the $25 \mu\text{m}$ pitch requires staggering or routing lines and $25 \times 100 \mu\text{m}^2$ is out of reach for most of the available non-indium BB options. The two foreseen cell sizes allow for the possibility to switch off 1/2 or 3/4 of the readout chip pixels (e.g. outer regions with pixel sensors of $100 \times 100 \mu\text{m}^2$ or $50 \times 200 \mu\text{m}^2$), whose advantages are presented in Sec. 3.2.

Figure 3. Principle sketch of the forward pixel geometry coverage under study. The “tile” geometry presents less coverage but also less overlap than the “petal” geometry.

3.2 Detector layout studies

The pixel detector is divided into barrel and forward geometries. The barrel sub-detector is foreseen to be instrumented with only two module types with 4×2 and 4×1 chips without a projective

hole at $z = 0$ (unpleasant feature present in the current detector). For the forward part two possible coverage schemes are being considered, called “tile” and “petals” as shown in Fig. 3. From simulations the “tile” geometry with module types 4×2 , 4×1 , and 2×2 has a coverage of 89% and an overlap of 12%, using 26 modules and 160 readout chips, while the “petal” geometry with 4×2 and 2×1 modules has a coverage of 98% and an overlap of 45%, using 44 modules and 232 readout chips (numbers are per disk and for a readout chip size of $21 \times 23 \text{ mm}^2$).

Figure 4. Studies of the pixel cell size for the forward and barrel geometries. All squared pixels, #2, should be ruled out because it has too high track impact parameter degradation, while the two opposite configurations, #1 and #5, have comparable tracking performance. Numbers are in μm and the colours of the numbers refer to the colours in the drawings.

Several barrel and forward pixel cell sizes and configurations have been studied. All tests are summarized in the sketch reported in Fig. 4. Tracking studies have been made for all configurations, pointing out that the configuration with all squared pixels, namely #2, presents too high track impact parameter degradation, while the two opposite configurations in terms of number of pixel cells, namely #1 and #5, have similar tracking performance, but configuration #5 requires about half the number of pixel cells of configuration #1 (see Fig. 5).

Figure 5. Tracking performance in terms of track impact parameter resolution for the two opposite pixel layout configurations. The plot on the left was made with the configuration having the higher number of pixel cells (#1), while the plot on the right was made with the configuration having the lower number of pixel cells (#5).

4. Readout chip specifications

The readout chip design presents huge challenges in terms of radiation hardness and hit rate ca-

pabilities. In Table 1 are reported the readout chip specifications for the current chip, the phase-I chip, and the phase-II chip in order to highlight the “quantum-step” in terms of design challenges that must be overcome in the phase-II chip design.

Table 1. Readout chip specifications for the current chip, the phase-I chip, and the phase-II chip.

Characteristics	CMS readout chip generations		
	Present	Phase-I	Phase-II
Pixel size	$100 \times 150 \mu\text{m}^2$	$100 \times 150 \mu\text{m}^2$	$50 \times 50 (25 \times 100) \mu\text{m}^2$
Sensor type	2D, 300 μm	2D, 300 μm	2D / 3D, thin
Chip size	$8 \times 10 \text{ mm}^2$	$8 \times 10 \text{ mm}^2$	$> 20 \times 20 \text{ mm}^2$
Transistors	1.3×10^6	1.6×10^6	$\sim 10^9$
Hit rate	100 MHz/cm ²	400 MHz/cm ²	$\sim 2 \text{ GHz/cm}^2$
Hit memory / chip	0.1 Mb	1 Mb	$\sim 16 \text{ Mb}$
Level-1 trigger rate	100 kHz	100 kHz	$\sim 750 \text{ kHz}$
Trigger latency	3.2 μs	3.2 μs	$\sim 12 \mu\text{s}$
Readout rate	40 Mb/s	400 Mb/s	$\sim 2 \text{ Gb/s}$
Radiation	15 Mrad, $r = 42 \text{ mm}$ $L = 150 \text{ fb}^{-1}$	120 Mrad, $r = 29 \text{ mm}$ $L = 500 \text{ fb}^{-1}$	$\sim 1 \text{ Grad}$, $r = 30 \text{ mm}$ $L = 3000 \text{ fb}^{-1}$
Technology	250 nm	250 nm	65 nm
Architecture	Analog	Digital	Digital
Buffer location	End Of Column	End Of Column	Pixel
Power consumption	$\sim 0.15 \text{ W/cm}^2$	$\sim 0.15 \text{ W/cm}^2$	$\sim 0.3\text{-}0.5 \text{ W/cm}^2$

Figure 6. Readout chip architecture conceptual design.

The readout chip architecture is sketched in Fig. 6. In particular the chip should have a threshold of at most $1000 e^-$ and a maximum capacitance of $\sim 100 \text{ fF}$ to keep the amplifier design simple. The chip should possess the possibility to tune the bias currents of the analogue front-end to account for different sensor choices, see Sec. 5. Moreover the digital hit processing, including the trigger latency buffer, should be implemented in pixel regions (e.g. 2×2 or 4×4 pixels), followed by data merging, formatting and readout after the first level trigger accept (the price of local digital

processing is that digital noise injection into the front end must be controlled, and clock and trigger signals must be distributed throughout the pixel matrix).

Figure 7. Readout chip data-link conceptual design.

Figure 7 shows the data-link capabilities that the readout chip should possess in order to effectively transmit the information to the backend electronics. In particular the chip should implement a data merging functionality (from 2 or even 4 chips in the innermost region), and it should provide up to 8 data output e-links of 1.3 Gb/s.

Some preliminary studies about radiation hardness had shown that, among other effects, PMOS-FETs (especially minimum size ones) show large transconductance degradation versus dose (the transconductance variation becomes very steep for a dose greater than 100 Mrad). The damage mechanisms have yet to be fully understood but it appears that some of the radiation damage in the chip could be annealed with high temperatures. This opens up the possibility to define plausible annealing scenarios during detector maintenance to optimize the longevity of both sensors and electronics (detailed evaluation of annealing effects on sensor performance have to be thoroughly studied). For a more specific discussion on this topic please refer to other proceeding articles from the same conference.

5. Possible sensor choices

The sensor candidate technology had been identified in planar silicon n-on-p (the n-on-p process is more cost effective than present n-on-n because it is a single-sided process). The details of the design, such as the thickness, the process (FZ, MCz, EPI), the spark rejection material, the pixel isolation, and the bias scheme, still have to be defined.

Thin planar sensor advantages have been thoroughly documented [5]. Such sensors present a higher field for the same bias voltage, which means a shorter drift time and therefore less trapping and, ultimately, a better radiation hardness. Moreover they also present a reduced full-depletion voltage, which in turn corresponds to smaller clusters allowing for a reduction of merged clusters in dense jets.

Figure 8 shows a comparison of full-depletion voltage as a function of annealing time between Magnetic Czochralski (MCz) and Float Zone (FZ) processes for planar sensors [6]. MCz is much more stable than FZ, which in turn implies that with MCz longer warm periods are possible. This might impact readout chip operations as described in Sec. 4. On the other hand the price for MCz material is expected to be higher than FZ material. Another possible sensor process which seems to be promising is epitaxial silicon (EPI). Indeed Fig. 9 shows bench and testbeam measurements for n-on-p EPI strip sensors (100 μm thick and with 80 μm pitch) irradiated up to

Figure 8. Full-depletion voltage as a function of annealing time for Magnetic Czochralski (MCz) and Float Zone (FZ) planar silicon sensors 200 μm thick.

3×10^{15} 1MeV eq.n. / cm^2 , in particular the noise is at a reasonable level, $\sim 700 \text{ e}^-$, if the sensor is kept at $\sim -20^\circ\text{C}$ and with an applied bias voltage of 800 V. In these conditions the charge collection efficiency reaches $\sim 80\%$.

Figure 9. Noise (left) and Charge Collection Efficiency (CCE, right) measurements on Epitaxial planar silicon sensors (EPI), 100 μm thick, irradiated at different fluences. The irradiated sensors are kept at -20°C (chips are at $+9^\circ\text{C}$), the non-irradiated sensors are kept at $+20^\circ\text{C}$ (chips are at $+24^\circ\text{C}$) [7].

An issue related to the n-on-p sensors is the generation of sparks between the sensor surface facing the readout chip (at high voltage) and the readout chip itself (at ground level potential). Possible solutions are under investigation. One possibility is to use Parylene-N (5-10 μm thick, deposited all over the module), for which it was demonstrated that it has no sparking up to 1000 V, no effect of irradiation up to 1×10^{16} 1MeV eq.n. / cm^2 , and it provides a good passivation. There are still some concerns about protection of bond pads during module manufacturing. An alternative material is the BenzoCycloButene (3 μm deposited with a lithographic process), for which it was demonstrated that it has no sparking up to 1000 V. It can be deposited before bump bonding at the IZM company, but radiation resistance measurements are still needed.

5.1 3D silicon sensors

For the innermost layers a radiation-harder technology is under investigation, the 3D silicon, for which is yet to be defined: the number of columns per cell, the column size and therefore the sensor thickness, the pad position, and the production process (single/double sided). Three companies manufacturing 3D silicon sensors have been identified: SINTEF, which offers a single-sided process, with passing-through columns and active edges (support wafer required); FBK, which offers a double-sided process, with full passing-through columns (full) and slim edges (200 μm);

Table 2. Laboratory and testbeam results from 200 μm thick FBK ATLAS08 batch and SINTEF (active edge $\sim 20 \mu\text{m}$). 1E, 2E, and 4E refer to the number of electrodes per pixel cell (fluence units are in $1\text{MeV eq.n.} / \text{cm}^2$).

Number of electrodes	Charge [$\phi = 0$]	Charge [$\phi = 7 \times 10^{14}$]	Charge Loss	Signal/Noise [$\phi = 0$]	Signal/Noise [$\phi = 7 \times 10^{14}$]
FBK ATLAS08					
1E	14.3 ke^-	8.2 ke^-	43%	66	33
2E	14.8 ke^-	10.5 ke^-	29%	55	38
4E	14.2 ke^-	11.8 ke^-	17%	36	32
SINTEF					
2E	17.2 ke^-	12.9 ke^-	25%	60	28

CNM, which offers a double-sided process, with partial passing-through columns and slim edges ($200 \mu\text{m}$).

Table 2 reports a comparison between two batches, FBK ATLAS08 and SINTEF, before and after irradiation up to $7 \times 10^{14} \text{ 1MeV eq.n.} / \text{cm}^2$. Best performance are given by the FBK ATLAS08 4E and the SINTEF 2E. Reference [8] shows that after irradiation the SINTEF sensors have a noise of $\sim 450 \text{ e}^-$, while the FBK ATLAS08 batch 2E and 4E have $\sim 280 \text{ e}^-$ and $\sim 350 \text{ e}^-$ respectively. The hit efficiency is comparable between the SINTEF and FBK ATLAS08 2E ($\sim 90\%$), while the FBK ATLAS08 4E has a lower efficiency, $\sim 80\%$ [8]. Further tests are under way in order to determine the best company and design.

5.2 Diamond sensors

An alternative sensor technology for the innermost layers that have proven a high radiation tolerance is CVD Diamond. For this technology several problems have still to be overcome, the more severe ones are the polarization effects. Though recent measurements show promising results for poly-crystalline sensors (pCVD) as reported in Fig. 10, where after irradiation up to $5 \times 10^{13} \text{ 1MeV eq.n.} / \text{cm}^2$ pCVD sensors show no pulse height dependence as a function of the rate, differently from the single-crystalline sensors (sCVD). Several studies are still needed to thoroughly understand the phenomena, for more details please refer to other proceeding articles from the same conference.

6. Conclusions

The operating conditions for the pixel detector after the high luminosity upgrade of LHC (HL-LHC) are extremely challenging, both in terms of radiation hardness and hit rate capabilities. The foreseen radiation fluence at 30 mm from the interaction point is $2 \times 10^{16} \text{ 1MeV eq.n.} / \text{cm}^2$, while the dose at the same distance will be 10 MGy (i.e. 1 Grad), and the hit rate is going to be $\sim 2 \text{ GHz/cm}^2$. The CMS collaboration is finalizing the general detector layout and geometry. The RD-53 ATLAS-CMS cross-collaboration is developing the main block of the readout chip in 65 nm CMOS technology for which the radiation hardness up to the foreseen 10 years of operation at HL-LHC has yet to be demonstrated. The sensor candidate technology is thin planar n-on-p silicon

Figure 10. Polarization effects on single-crystalline (sCVD, left) and poly-crystalline (pCVD, right) Diamond sensors after irradiation up to 5×10^{13} 1MeV eq.n. / cm^2 . Different curves correspond to different particle rates. pCVD Diamond sensors do not show any pulse height dependence as a function of the rate.

(and/or silicon 3D, or Diamond, for the innermost layers) for which several bench and testbeam studies are under way in order to determine the best design.

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