Pixel front-end development in 65 nm CMOS technology

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Pixel front-end development in 65 nm CMOS technology

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ABSTRACT: Luminosity upgrade of the LHC (HL-LHC) imposes severe constraints on the detector tracking systems in terms of radiation hardness and capability to cope with higher hit rates. One possible way of keeping track with increasing luminosity is the usage of more advanced technologies. Ultra deep sub-micron CMOS technologies allow a design of complex and high speed electronics with high integration density. In addition, these technologies are inherently radiation hard.

We present a prototype of analog pixel front-end integrated circuit designed in 65 nm CMOS technology with applications oriented towards the ATLAS Pixel Detector upgrade. The aspects of ultra deep sub-micron design and performance of the analog pixel front-end circuits will be discussed.

KEYWORDS: Analogue electronic circuits; Front-end electronics for detector readout; VLSI circuits

1 Corresponding author.
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## 1 Introduction

In 2022, luminosity of the Large Hadron Collider (LHC) will be increased by the factor of ten from the nominal luminosity of $10^{34} \text{cm}^{-2}\text{s}^{-1}$ to $10^{35} \text{cm}^{-2}\text{s}^{-1}$ [1]. The existing particle tracking systems were not designed to operate in the high luminosity environment where the innermost tracking layers have to be radiation tolerant up to 1000 Mrad and deal with particle hit rates of about 1 GHz/cm$^2$. In order to keep a good tracking performance, new technologies have to be used. Ultra deep sub-micron technologies offer inherent radiation hardness and allow a high integration density. However, smaller transistors are more susceptible to mismatch and low power supply voltage can negatively impact analog performance of the front-end electronics.

To explore the analog performance of the pixel front-end electronics designed in 65 nm CMOS technology, two prototype integrated circuits have been designed: FE-T65-0 and more advanced FE-T65-1. FE-T65-0 is a basic demonstrator chip. By evaluating the properties of the FE-T65-0, valuable lessons have been learned and used in design of more advanced FE-T65-1. Therefore, the results of FE-T65-0 testing will be mentioned briefly and FE-T65-1 will be described in more detail. Both chips have been characterized without sensors.

## 2 FE-T65-0

FE-T65-0 is a prototype integrated circuit consisting of the basic building blocks of an analog front-end read-out chain: charge sensitive amplifier (CSA) and comparator. Two versions of the CSA with switched reset and two different feedback capacitances (3 fF and 5 fF) are followed by either continuous or dynamic comparator. The design of a single pixel is shown in figure 1. The dimensions of a single analog front-end (CSA and comparator) are very small -36×25 μm$^2$, and therefore it can be easily integrated in a small pixel. Functionality of both versions of the CSA
has been successfully demonstrated. The noise performance has been determined with a threshold scan and fitting the resulting s-curve by error function and evaluated in terms of Equivalent Noise Charge (ENC). The versions of the analog front-end with the continuous comparator have relatively low noise of about 75 electrons. Noise of the version with the dynamic comparator could not be meaningfully determined due to the problem with the dynamic comparator exhibiting large offset of about 100 mV. The problem is related to the fact that the comparator uses four transistors stacked in one current branch as shown in figure 2, and due to the small power supply voltage of 1.2 V they do not operate properly. Upon these results from testing of the FE-T65-0 we designed a new, more advanced chip FE-T65-1 to reduce the offset of the dynamic comparator and also implement a tunable input capacitance to study the noise performance in more realistic conditions - as in presence of a pixel sensor.

3 FE-T65-1

FE-T65-1 is a pixel array consisting of 32 pixels with four different versions of the analog front-end electronics. These four versions are described in table 1. The layout of the FE-T65-1 is illustrated in figure 3 and the layout of a single pixel is shown in figure 4.

Two versions of the CSA have been implemented in FE-T65-1: CSA with continuous reset and CSA with switched reset. Both versions of the CSA are based on a single stage architecture implemented with a telescopic cascode with divided current sources. The firstly mentioned version
Figure 3. Layout of the FE-T65-1. Four versions of the analog pixel front-end electronics with 32 pixels in total are integrated on the silicon chip with dimensions of $1 \times 1 \, \text{mm}^2$.

Figure 4. Layout of a single pixel of the FE-T65-1. Pixel size is $180 \times 25 \, \mu\text{m}^2$.

of the CSA uses a current source in the feedback loop establishing a linear discharge and thus providing a characteristic triangular signal shape. This architecture is advantageous for providing information about the signal charge in terms of Time Over Threshold (ToT). A disadvantage of this architecture is long discharge time (several LHC bunch-crossings) and ballistic deficit. The switched version of the CSA has a switch in the feedback loop allowing an instantaneous discharge of the CSA. Signal can be injected and reset within one LHC bunch crossing (25 ns). However, this fast operation requires more power. The switched version CSA can not be used for a ToT measurement. FE-T65-1 contains pixels with two types of comparators: continuous and dynamic. The continuous comparator operates asynchronously while consuming power all the time. The dynamic comparator is clocked and is active only on the rising edge of the clock signal. Its static power consumption is negligible and dynamic power consumption scales linearly with frequency. The schematics of the continuous and the dynamic comparators are shown in figures 5 and 6.

Apart from the CSA and the comparator, the analog part of the pixel contains a 4-bit DAC (FDAC) for the CSA discharge current adjustment and a 5-bit DAC (TDAC) for adjusting the threshold voltage of the comparator. All pixel versions also contain a bank of three capacitors.
which can be switched to the input node of the CSA. These capacitors are implemented as parasitic inter-metal capacitors and they cover input capacitance range from almost 0 to 175 fF. All pixel versions have identical digital part implementing a 8-bit counter and a 15-bit configuration register.

4 Noise versus capacitance

Noise of the pixel electronics within the FE-T65-1 has been determined by a threshold scan performed in the same way as in the case of FE-T65-0 and plotted as a function of two quantities having the greatest impact on the noise performance: input capacitance of the CSA ($C_{IN}$) and bias current of the input transistor $I_{BIAS}$. The results for each version are shown in figures 7–10. Comparing the pixel versions in terms of noise, the versions with the dynamic comparator (versions 2 and 4) exhibit systematically higher noise than the versions with the continuous comparator (versions 1 and 3). This effect can be attributed to the fact that periodical switching of the dynamic comparator generates additional digital activity in the pixel which couples to the sensitive analog part. Another difference in noise figures have been observed between versions of the CSA. The switched CSA has systematically lower noise than the continuous CSA. This difference in noise performance can be explained by different transistor dimensions of the continuous and switched CSA and also by different bias conditions. In addition, absence of the continuous current source in the feedback loop of the switched CSA is in favour of lower noise of the switched CSA. Operation frequency of the switched versions was 40 MHz. The average ENC of all pixels of each version is summarized in table 2.

Noise measured at a constant bias current is linearly dependent on the input capacitance. This

![Figure 5](image1.png)  \[\text{Figure 5. Schematic of the continuous comparator.}\]

![Figure 6](image2.png)  \[\text{Figure 6. Schematic of the dynamic comparator.}\]

![Table 2](table.png)

Table 2. Mean noise and power consumption of all versions of the analog pixel electronics implemented in the FE-T65-1.

<table>
<thead>
<tr>
<th>Version</th>
<th>CSA</th>
<th>Comparator</th>
<th>$\langle\text{ENC}\rangle$ [e$^-$]</th>
<th>P [µW]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Continuous</td>
<td>Continuous</td>
<td>144</td>
<td>10.4</td>
</tr>
<tr>
<td>2</td>
<td>Continuous</td>
<td>Dynamic</td>
<td>183</td>
<td>10.6</td>
</tr>
<tr>
<td>3</td>
<td>Switched</td>
<td>Continuous</td>
<td>113</td>
<td>14.6</td>
</tr>
<tr>
<td>4</td>
<td>Switched</td>
<td>Dynamic</td>
<td>157</td>
<td>14.8</td>
</tr>
</tbody>
</table>
behavior agrees with a general analytical model of a charge sensitive amplifier described for example here [2], as well as with noise simulations. Therefore, sensor type and pixel geometry (resp. sensor capacitance) will play a central role in the noise performance of the new pixel detector. More detailed studies of the pixel sensor capacitance can be found here [3].

5 Dynamic performance and power consumption

Dynamic performance of the front-end electronics has been studied in terms of timewalk-signal dependent delay between charge injection and receiving a hit at the output of the comparator. Significant timewalk has been observed in version 1. When the signal is close to the threshold (2 000 electrons), the comparator fires 35 ns later than in case of a large signal (40 000 electrons), as shown in figure 11. This unwanted effect can cause assignment of the hit to the wrong bunch crossing. The timewalk can be reduced by increasing the bias current of the CSA and the comparator and thus speeding up the electronics. The timewalk drops below 25 ns when power consumption is increased from the original 10.4 µW to 18 µW. Significant elimination of the timewalk has been achieved with the dynamic comparator in version 2.
Figure 11. Timewalk of version 1 for two different bias currents of the CSA.

Table 3. Threshold dispersion before and after threshold tuning of the four pixel versions in the FE-T65-1.

<table>
<thead>
<tr>
<th>Version</th>
<th>CSA</th>
<th>Comparator</th>
<th>Disp. before tuning [e⁻]</th>
<th>Disp. after tuning [e⁻]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Continuous</td>
<td>Continuous</td>
<td>267</td>
<td>22</td>
</tr>
<tr>
<td>2</td>
<td>Continuous</td>
<td>Dynamic</td>
<td>405</td>
<td>28</td>
</tr>
<tr>
<td>3</td>
<td>Switched</td>
<td>Continuous</td>
<td>272</td>
<td>20</td>
</tr>
<tr>
<td>4</td>
<td>Switched</td>
<td>Dynamic</td>
<td>298</td>
<td>21</td>
</tr>
</tbody>
</table>

Contribution of the dynamic comparator to the total timewalk is negligible, and therefore version 2 can operate with the nominal power consumption of 10.6 µW with timewalk smaller than 25 ns. Since the switched versions operate with frequency of 40 MHz, timewalk is not an issue here, but the nominal power consumption is higher - about 14.7 µW.

6 Threshold dispersion

Variations of fabrication process and a mismatch of transistor dimensions across the chip cause dispersion of the comparator threshold between channels in the pixel matrix. In order to compensate for this effect, a 5-bit DAC has been integrated in each pixel to locally tune the threshold voltage. The threshold dispersion of each version has been measured before and after threshold tuning and the results are summarized in table 3.

Example of a s-curve distribution of 8 pixels of the pixel version 1 before tuning is shown in figure 12 and after tuning in figure 13. In all versions we were able to tune the threshold dispersion below 30 electrons. However, the versions with the dynamic comparator suffer from higher threshold dispersion before tuning due to the higher sensitivity of the dynamic comparator to the transistor mismatch. We have to note that our design contains only 8 pixels of each version, which does not allow us to make larger statistics about threshold dispersion. In a large chip (100 000 pixels), the final threshold dispersion can be higher.
7 Summary

Two prototypes of integrated circuits of a pixel front-end electronics have been designed in 65 nm CMOS technology and tested. No principal show stopper has been found for using the 65 nm CMOS technology for implementation of the analog part of a pixel front-end chip. The overall analog performance of FE-T65-1 is at least comparable with the latest version of the ATLAS pixel front-end chip FE-I4 [4] designed in 130 nm CMOS technology. A similar prototype chip designed in 65 nm CMOS technology has been independently developed by a research group in Lawrence Berkeley National Laboratory [5]. Their test results also indicate a good analog performance, as well as good radiation hardness.

Acknowledgments

Special thanks belong to W. Dietsche and W. Ockenfels for wire-bonding of both prototype chips to test PCBs. This project has been supported by the German Ministerium für Bildung, Wissenschaft, Forschung und Technologie (BMBF) under contract no. 05H2012PD1.

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