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GOSSIPO-4: Evaluation of a Novel PLL-Based TDC-Technique for the Readout of GridPix-Detectors

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Abstract—The direct readout of Micro-Pattern Gaseous Detectors (MPGDs) with bare pixel chips introduces the need for a new generation of readout electronics featuring a high spatial granularity as well as a highly accurate time measurement in each pixel. GOSSIPO-4, fabricated in a 130 nm CMOS technology, is a demonstrator ASIC investigating the potential of a new TDC-concept that is based on a chip-wide 40 MHz clock which is complemented by an additional 640 MHz clock. The latter is created upon demand by local oscillators distributed across the pixel matrix. PLL tuning of the local oscillators allows for automatic compensation of frequency fluctuations caused by process parameter, supply voltage and temperature variations. The developed PLL locks within 4 μ s and achieves a duty cycle of 50.75% with a time interval error of only 23.4 ps. Mean DNL and INL of the TDC are less than 20% of the time bin size of 1.56 ns under all anticipated conditions.

Index Terms—Gaseous detectors, GOSSIP, gridpix, high-accuracy TDC, InGrid, micromegas, MPGDs, timepix.

I. INTRODUCTION

THE readout of Micro-Pattern Gaseous Detectors (MPGDs) by means of bare pixel chips instead of the conventionally used pad-planes was pioneered in 2004 [1], [2]. Since then, this concept has been successfully applied in TPC-prototypes [3], [4], photoelectric X-ray polarimetry [5] and rare particle searches [6].

The maximal detector integration is achieved in GridPix-detectors utilizing Micromegas [7] for signal amplification in the gas-phase. The operation principle of such detectors is illustrated in Fig. 1(a): Electron-ion pairs are created in the drift region by incident ionizing radiation. An electric field of up to several kV/cm causes the ions and electrons to move towards the cathode and the readout anode, respectively. The latter is made of the integrated amplification grid, the so-called InGrid-structure [8], [9] depicted in Fig. 1(b)), and a pixelized readout ASIC. Underneath the amplification grid, the applied electric

Fig. 1. (a) Operation principle of a GridPix-detector [4]. (b) Scanning micro-scope picture of an InGrid structure [10]. The amplification grid is supported by SU-8 pillars which are hidden inbetween the grid-holes. The latter are aligned with the pixels of the ASIC underneath.

field reaches several 10 kV/cm. Hence, an electron avalanche is triggered by each primary electron entering this region, thus, enabling signal detection by the pixels of the ASIC. Since the distance covered by the drifting electrons is directly proportional to the drift-time, the 3-dimensional coordinates of the primary ionizations are easily reconstructed from the positions of the hit pixels and the measured arrival time of the hit. In transverse direction, the achievable single-point resolution is predetermined by the pixel size, while it is limited by the accuracy of the drift-time measurement in longitudinal direction.

Improving the circuitry tested on GOSSIPO-3 [11], [4], the GOSSIPO-4 demonstrator discussed in this paper is the final prototype for Timepix3 [12] – the full featured successor of the Timepix ASIC [13] which was utilized in several previous studies validating the GridPix detector concept. The paper is organized as follows: The TDC-technique is described in Sec. II. The circuitry implemented on the demonstrator-chip is presented in Sec. III, the focus is here on the Phase Locked Loop (PLL) which ensures the high TDC accuracy. Before the conclusions are drawn in Sec. V, the achieved PLL- and TDC-performance are discussed in Sec. IV.

II. THE TDC-TECHNIQUE

In order to provide the required single point resolution in longitudinal direction, the Time of Arrival (ToA) of individual charge depositions has to be measured with a precision of a few nanoseconds in GOSSIP-detectors (acronym for: Gas On Slimmed Silicon Pixels, denoting GridPix detectors made of slimmed silicon chips. This concept is evaluated for the ATLAS upgrade [14]). In principle, this can be achieved with the TDC-

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Fig. 2. Timing diagram of GOSSIPO-4. Two subsequently running counters are used for the ToA measurement. The length of the hit signal (Time-over-Threshold or ToT) is a measure for the input charge.

technique known from the Timepix ASIC by simply increasing the clock frequency to several 100 MHz. However, due to the high demands on signal routing and power supply as well as on cross-talk suppression, a chip wide high frequency clock network is highly undesirable on a mixed-signal ASIC.

The TDC-technique introduced in [15] circumvents these issues by creating the high-frequency clock locally in the pixels only when it is needed, see Fig. 2 for a timing diagram. When the discriminator in a pixel senses a hit, a 640 MHz ring-oscillator located next to that pixel is enabled. The number of fast clock cycles until the occurrence of the first rising edge of the chip wide slow-clock (40 MHz) is counted with a Linear Feedback Shift Register (LFSR). Then the ring-oscillator is stopped and the number of slow clock cycles until the end of the acquisition window is counted. The ToA with respect to the end of the acquisition window can be calculated from the number of counted fast and slow clock cycles (n_{fast} and n_{slow}) and the corresponding frequencies (f_{fast} and f_{slow}):

$$ToA = - \left(\frac{n_{fast}}{f_{fast}} + \frac{n_{slow}}{f_{slow}} \right). \quad (1)$$

Since the ring-oscillators are operated only for short time intervals, neither synchronization between the individual oscillators nor long term stability are an issue. However, as can be seen in [15], the absolute oscillation frequency has to be tuned due to frequency variations caused by inaccuracies in the production process. In [4], it has been found that tuning Voltage Controlled Oscillators (VCOs) by an on-chip Low DropOut Regulator (LDO) as done on GOSSIPO-3 is a feasible but not the ideal technique for such frequency tuning. On GOSSIPO-4, the VCOs are, consequently, replaced by the circuit described in Section III-B.

III. GOSSIPO-4 CIRCUITRY

GOSSIPO-4 is a demonstrator IC meant to verify that above described TDC-technique performs well when RC-controlled oscillators that are distributed across a pixel matrix are automatically tuned by a PLL in the chip periphery. The chip is produced in a 130 nm technology and operated at 1.5 V. For testing purposes, it carries a PLL which provides the oscillator control voltage and the digital part of 8 pixels organized in a $55 \mu\text{m}$ -pitch forming a so-called super-pixel. This layout resembles the structure of the succeeding Timepix3 which will feature 256×256 pixels organized in 8192 super-pixels.

Fig. 3. Block diagram of the GOSSIPO-4 super-pixel.

A. The Super-Pixel

The logic implemented in the pixels forming the GOSSIPO-4 super-pixel is sketched in Fig. 3. The 8 individual pixels of the super-pixel share one ring-oscillator which is enabled upon pixel activation. One of four available test-inputs can be logically interconnected with the counting- and synchronization-logic which controls the operation of the two ToA- and the Time-over-Threshold- (ToT-) counters of a pixel. These test-inputs mimic the signal of the pixel front-end in a fully operational ASIC and allow activation of different pixels at arbitrary times.

Neglecting the parasitic influence of the time-walk effect introduced by front-end electronics, this setup allows to determine the accuracy which can be maximally achieved with the proposed TDC-technique. In case of the Timepix3 ASIC, the limitations introduced by the time-walk effect are addressed by fast analog circuitry and, using the ToT information on the input charge, by a time-walk compensation technique during data analysis.

The implemented counters with 2^n states are LFSRs following the De Bruijn technique [16]. The counting logic is a synchronous 3 bit finite-state machine which controls the counters during the data taking and the readout phase. Besides by the 40 MHz clock, it is externally controlled by three signals: Reset, Trigger and Token.

The synchronization logic is an asynchronous state machine that creates a gate-signal starting with the hit-signal and stopping at the first rising edge of the system clock. This gate-signal enables the local oscillator if necessary and synchronizes the fast clock signal with the system clock. Thus, glitches compromising correct counter operation are suppressed.

B. The RC-Controlled Ring-Oscillators

The schematic of the GOSSIPO-4 ring-oscillators is shown in Fig. 4. Variation of the control voltage U_{ctrl} allows for tuning of the oscillation frequency since the varactor capacitances and, hence, the RC-times of the delay elements are voltage dependent. Since it is basically an unloaded static potential, distribution of the control voltage across the pixel matrix is easier than in the previous approach discussed in [11], [4].

The target frequency of 640 MHz can be reached in all process corners, see Fig. 5. As seen from Monte Carlo simulations, the output frequencies vary by less than 1% from one

Fig. 4. The ring-oscillators on GOSSIPO-4 are made of 4 daisy-chained inverters with voltage controllable RC-elements in between.

Fig. 5. Oscillator frequency in dependence on the control voltage (simulations). Different process corners are shown together with the target frequency of 640 MHz. The latter is reached in all corners.

Fig. 6. Creation and distribution of the oscillator control voltage.

oscillator to another on the same die due to the good resistor and capacitor matching properties.

C. The PLL Architecture

The oscillator control voltage is generated by means of a PLL and will be broadcasted across the super-pixel matrix of a fully-fledged pixel chip for adjustment of the oscillation frequencies, as shown in Fig. 6. This approach allows to compensate in all pixels for frequency fluctuations caused by supply voltage or process parameter variations as well as for temperature changes with a single PLL in the chip periphery.

The developed PLL is based on the work presented in [17]. It is made of a Phase-Frequency-Detector (PFD), a charge-pump, a third-order passive loop-filter, a copy of the RC-controlled

Fig. 7. Schematic of the phase-frequency detector. The ref_{fast} and fb_{fast} signals are available off-chip for monitoring purposes.

oscillator which is instantiated in the super-pixel and a clock divider. The functional blocks are described in some detail in the following.

Phase Frequency Detector: The PFD detects phase and frequency differences between the input reference clock (clk_{ref}) and the feedback clock signal (clk_{fb}). As shown in Fig. 7, the PFD consists of two resettable, positive edge triggered D-flip-flops, an AND-gate and a delay cell. The inputs of both flip-flops are tied to the vdd -level.

The functionality is that of a state machine with three states: If the reference clock leads the feedback clock, the up -signal goes high while the $down$ -signal remains low. If the feedback clock leads the reference clock, a high pulse appears in the $down$ -signal while the up -signal remains low. If input phase and frequency are equal the PLL is locked at the correct frequency. In this case, very narrow pulses appear at the up - and $down$ -signals.

A dead-lock can occur when the phase-error becomes small in comparison with the combined response time of PFD, charge-pump, and the loop-filter. This causes the phase detector gain to drop to zero, which in turn prevents further frequency adjustments. In order to avoid this dead-lock, the delay on the PFD reset path is made larger than the switching time of the charge pump currents. Besides, the delay time τ_1 has to be optimized for an ideal trade-off between the linearity and in-band noise of the charge pump.

The output of the other two D-flip-flops (ref_{fast} and fb_{fast}) track the up - and the $down$ -signals with a delay τ_2 , hence, realizing a lock-detection circuit whose output is made available off-chip. The value of the delay time τ_2 determines the sensitivity of the loss of lock detection, it has to be chosen relatively large with respect to τ_1 in order to give an accurate representation of the lock status.

Charge-Pump: The charge pump uses a differential architecture with a dummy branch (see Fig. 8). The two switched current sources charge or discharge the capacitor C_1 of the loop-filter with $80 \mu A$ (configurable), thus, converting the phase and frequency differences into a control-voltage. The branches are controlled by the up - and $down$ -, the $\overline{up}$ - and $\overline{down}$ -signals, respectively. The transistors (M5, M6 and M8) form current mirrors providing the biasing current for the charge pump. For

Fig. 8. Schematic of the charge-pump and the loop-filter.

charge-sharing minimization, the switch transistors (M1-M4) in the charge pump are minimum size.

Loop-Filter: As discussed in [18], the third-order loop-filter shown in Fig. 8 eliminates undesired high frequency noise signals and, therefore, ensures a stable control voltage. It consists of two resistors (R_1 and R_2) and three capacitors (C_1 , C_2 and C_3) that create a three-pole one-zero network. Adequate selection of these parameters allows for optimization of the noise performance and circuit stability. Based on system-level simulations, C_1 , introducing low-pass characteristic to U_{cp} , has been fixed at 710 fF. C_2 and R_1 , largely determining the PLL stability, were fixed at 7.4 pF and 22 k Ω , respectively. The third branch of the loop filter (C_3 and R_2) forms another non-dominant frequency pole that further filters high frequency noise on the control voltage U_{ctrl} . In order to meet the requirements on area and suppression performance, C_3 and R_2 have been chosen to be 320 fF and 11 k Ω , respectively.

Frequency-Divider: The frequency divider is made of a chain of four D-flip-flops dividing the oscillator output frequency of 640 MHz by 16, hence, yielding the needed 40 MHz feedback-clock.

SLVDS-Driver: A Scalable Low Voltage Differential Signal (SLVDS) driver as shown in Fig. 9 has been designed enabling off-chip investigation of a 320 MHz clock signal which can be used for characterization of the PLL. The chosen differential transmission scheme is insensitive to common-mode signal disturbances and crosstalk. Therefore, it allows to operate at small signal levels without a reduction of the noise margin.

As proposed in [19], the driver implementation is based on a four-transistor switching scheme arranged in a bridge configuration. When the transistors M10 and M12 are switched off, the transistors M11 and M13 are switched on and the polarity of the output current is positive and vice versa. The choice of the dimensions of the switching transistors M10-M13 is made trading on-resistance for power consumption. A small on-resistance is

Fig. 9. Schematic of the SLVDS driver.

desired to get a small voltage-drop across the switching transistors. It is achieved when wide transistors are implemented. This in turn increases the capacitive load introduced by the transistor gates and, eventually, the power consumption.

The common-mode voltage is sensed by means of a high-ohmic voltage divider formed by the resistors R_4 and R_5 . It is fed-back to the differential pair formed by the transistors M22 and M23 where it is compared to the applied offset voltage V_{os} . The biasing voltage of the NMOS-transistors M14-M16 and the PMOS-transistors M17-M19 is controlled by the common-mode feedback such that the applied offset voltage V_{os} is enforced. The feedback-loop is stabilized by a pole-zero compensation network formed by R_6 and C_5 .

The signal current and thereby the power consumption can be controlled by setting the configuration bits controlling the gates of the transistors M14-M19. The NMOS-gates can be switched either to the biasing voltage provided by transistor M20 or to ground potential. The gates of the PMOS-transistors can be biased either with the voltage provided by transistor M21 or the supply voltage, v_{dda} .

IV. MEASUREMENT RESULTS

For measurements on the PLL- and the TDC-performance, the chip was bonded to a standard chip package and mounted on a printed circuit board, as shown in Fig. 10. The logic stimuli needed for operation as well as the readout of the data are provided by a Spartan-3 FPGA hosted on the multipurpose S3-MultiIO-board developed at the University of Bonn [20].

A. PLL Performance

For the measurements on the PLL performance, the 40 MHz reference clock is provided by an Agilent 81134A signal generator. The outputs of the on-chip LVDS driver are directly connected to a differential probe of a Tektronix MS-O70804 oscilloscope (25 GS/s, 8 GHz bandwidth). The S3-MultiIO-board is used only as power supply.

The Time Interval Error (TIE) defines how far each active edge of the output clock varies from its ideal position. A jitter

Fig. 10. Photograph of the test-setup showing the S3MultiIO board (left) and the dedicated GOSSIPO-testboard (right).

Fig. 11. Time Interval Error (TIE) at the 320 MHz output.

histogram for a TIE measurement is shown in Fig. 11. Fitting by a Gaussian distribution yields a width (σ) of only 23.4 ps.

Fig. 12 shows an eye diagram of the 320 MHz output clock. Besides the central branch, two side-branches caused by cross-talk from the positive and the negative edge of the reference clock are observed in this plot. This is no issue of the PLL itself, but only of the present test-chip on which the reference-clock and the LVDS-wire-bond pads are located next to each other. The total eye-opening is 1.37 ns on the time axis and about 340 mV on the voltage axis. The main PLL characteristics are listed in Table I.

B. TDC Delay-Scan

A diagram of the setup used for TDC characterization is shown in Fig. 13. The Qt-based DAQ controls an Agilent 81110A pulse generator and the S3-Multi-IO-board which provides the necessary logic stimuli for operation and read-out of the super-pixel.

The most important measurement is a delay-scan performed by activating the test-inputs at well defined times relative to the

Fig. 12. Eye diagram of the output frequency of 320 MHz.

TABLE I
PLL CHARACTERISTICS

total PLL area	208 $\mu\text{m} \times 106 \mu\text{m}$
jitter performance (TIE)	23.4 ps at 320 MHz output
cycle-to-cycle jitter	50.4 ps at 320 MHz output
period jitter	31.2 ps at 320 MHz output
duty cycle	50.75 %
power consumption	$\approx 4 \text{ mW}$
time to lock	4 μs
VCO output frequency range	490 – 740 MHz

Fig. 13. Block diagram of the setup used for investigation of the TDC performance.

reference clock. The applied delays range from 0 ns to 40 ns in 0.1 ns steps. For each delay, 1000 pixel activations have been performed. The fast counter values observed in a full delay-scan of pixel 0 on chip 1 are depicted in Fig. 14.

The individual TDC-bins are characterized by their widths Δt_i , given by $t_{\text{max},i} - t_{\text{min},i}$ which are start- and end-point of a time-bin, as well as by σ , the steepness of the edges which is proportional to the time jitter. These parameters are obtained by matching (complementary) Gauss error functions:

$$f(t) \propto \int_t^{\infty} e^{-\frac{(t-t_{\text{min}})^2}{2\sigma_{\text{min}}^2}} dt \quad (2)$$

to the data. See Fig. 15 for an example plot of a typical TDC-bin.

Fig. 14. Result of the delay-scan described in Sec. IV-B: Test pulses sent with specific delays are measured in the corresponding fine ToA bin. Only values of the fast counters are shown.

Fig. 15. Example of a fit performed on bin 2 of the TDC. The matched twofold error function eq. (2) is shown as continuous line over the dashed histogram.

The differential non-linearity (DNL) is calculated from the actual and the ideal TDC-bin width, Δt_i and $\Delta t_{\text{theo.}} = 1.56$ ns, respectively:

$$DNL_i = \frac{\Delta t_i - \Delta t_{\text{theo.}}}{\Delta t_{\text{theo.}}} \quad (3)$$

The DNL quoted for a specific TDC is the maximum of all individual absolute DNL_i values of this TDC.

The integral non-linearity (INL) is given by the maximum deviation from the ideal TDC-characteristics:

$$INL = \max \left[\sum_{i=0}^j DNL_i \right]_{j=1 \dots N} \quad (4)$$

Characterization of Individual Pixels: The spread of the observed TDC-bin sizes is visualized in Fig. 16. The error-bars represent the jitter of the individual bins. It is rather low since only digital circuitry is investigated.

DNL and INL of all pixels on chip 1 are listed in Table II. It has to be noted that both DNL and INL are driven by the width of the second TDC-bin which shows the largest deviation from the ideal value. Since this is the first non-zero value, it is

Fig. 16. Dispersion of the TDC-bin sizes of pixel 0 on chip 1. The ideal bin size is drawn as dashed line. The error-bars show the jitter of the individual bins.

TABLE II
DNL AND INL FOR THE PIXELS ON CHIP 1

Pixel	DNL [ps]	INL [ps]
0	270	230
1	190	190
2	180	180
3	210	150
4	240	330
5	210	180
6	180	220
7	250	300

assumed that this effect is introduced by the start-up behavior of the ring-oscillator.

For all 80 investigated pixels on 10 different chips, similar results have been obtained. The mean DNL of all investigated pixels is 300 ps with a RMS of 80 ps. The INL is distributed around a mean of 380 ps with a RMS of 130 ps.

Characterization of Multiple Pixels in the Same Super-Pixel: In any application, it has to be anticipated that several pixels of one super-pixel are activated within a few nano- or even picoseconds. Whether or not this deteriorates the TDC performance is investigated by enabling all pixel in a super-pixel during the delay-scan. The result of this delay-scan performed with chip 1 is shown in Fig. 17. Some events which do not match the expectation are observed. This is only observed on chip 1 and the number of outliers is negligible. Consequently they are not taken into account for analysis. TDC-bin width and jitter are displayed in Fig. 18. Measured DNL and INL are listed in Table III.

The mean DNL of all investigated pixels is 330 ps with a RMS of 90 ps. The INL is distributed around a mean of 300 ps with a RMS of 100 ps. Concluding, it is stated that the DNL is not influenced if multiple pixels in one super-pixel are activated at the same time. The INL is even improved since the impact of the ring-oscillator start-up behavior does not affect pixels which start counting when the oscillator is already running.

Dependence on Power Supply Stability: Considering application in a full featured GOSSIP-detector, it has to be ensured that the TDC performance is not affected by perturbations on the power supply rail.

As intended, the PLL compensates for global variations of the supply voltage by readjusting the control voltage of the ring-oscillators. See Fig. 19 for a display of the control voltages in a

Fig. 17. Result of a delay-scan during which all pixels on chip 1 have been activated. The results of all pixels are superimposed. Only values of the fast counters are shown.

Fig. 18. Dispersion of the TDC-bin sizes of pixel 0 on chip 1. The ideal bin size is drawn as dashed line. All pixels of the super-pixel are activated at the same time. The error-bars show the jitter of the individual bins.

TABLE III
DNL AND INL VALUES FOR THE PIXELS OF CHIP 1. ALL THE PIXELS HAVE BEEN ACTIVATED AT THE SAME TIME

Pixel	DNL [ps]	INL [ps]
0	140	150
1	240	260
2	130	350
3	180	180
4	240	180
5	160	530
6	180	200
7	210	170

wide supply voltage range. On all chips, TDC operation is not compromised down to a supply voltage of 1.3 V.

As seen from a comparison of Figs. 16, 18, and 20, TDC-bin size dispersion and jitter are virtually not affected by a reduced supply voltage. Also DNL and INL are largely independent on power supply variations.

V. CONCLUSION

The GOSSIPO-4 demonstrator IC, fabricated in a 130 nm process, has been designed for verification of a novel PLL-based TDC-technique with nanosecond accuracy: A 640 MHz clock signal, providing high TDC accuracy, is created by a ring oscillator in the pixel matrix. The frequency of all oscillators in a full scale pixel chip is automatically tuned by a PLL in the chip periphery.

Fig. 19. Control voltage U_{ctrl} in dependence on the supply voltage (vdd) for the investigated chips.

Fig. 20. Dispersion and jitter (represented by the error bars) of the TDC bin sizes for pixel 0 on chip 1 at different supply voltages. The ideal bin size is drawn as dashed line.

In this paper, this approach has been verified: In each pixel, the TDC bin size is found to be about 1.56 ns. Differential and integrated non-linearity are less than 400 ps. At an 320 MHz test-output, the TIE jitter performance of the implemented PLL is below 24 ps, the duty cycle is 50.75%. Based on this success, Timepix3 featuring 256×256 charge sensitive pixels is designed using the central building blocks of the GOSSIPO-4 IC for time of arrival measurements.

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