The charge pump PLL clock generator designed for the 1.56 ns bin size time-to-digital converter pixel array of the Timepix3 readout ASIC

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The charge pump PLL clock generator designed for the 1.56 ns bin size time-to-digital converter pixel array of the Timepix3 readout ASIC

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ABSTRACT: Timepix3 is a newly developed pixel readout chip which is expected to be operated in a wide range of gaseous and silicon detectors. It is made of 256 × 256 pixels organized in a square pixel-array with 55 µm pitch. Oscillators running at 640 MHz are distributed across the pixel-array and allow for a highly accurate measurement of the arrival time of a hit. This paper concentrates on a low-jitter phase locked loop (PLL) that is located in the chip periphery. This PLL provides a control voltage which regulates the actual frequency of the individual oscillators, allowing for compensation of process, voltage, and temperature variations.

KEYWORDS: Analogue electronic circuits; Gaseous detectors; Hybrid detectors; CMOS readout of gaseous detectors

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1 Introduction

The Timepix3 predecessor, labeled Timepix [1], originated from the successful Medipix2 [2] ASIC developed at CERN. It was operated as active anode in various gaseous detectors with gas electron multipliers (GEMs) and MICROMEGAS [3] for gas amplification. Such charge collection on the bare pixels of a specially developed ASIC is one of the readout concepts pursued for a TPC operated at a future linear collider. However, this application demands for several improvements now implemented in the recent Timepix3 ASIC. The Timepix3 readout chip was designed by a collaboration of CERN, NIKHEF, and the University of Bonn. It features an active surface of $1.4 \times 1.4 \text{ cm}^2$. Each pixel contains an analog front end: a charge sensitive amplifier, a discriminator and a 4-bit digital-to-analog converter for threshold adjustment. Signals of positive and negative polarity can be processed. The digital part of the pixel includes a 10-bit time-over-threshold counter, a 14-bit coarse time-stamping register and a 4-bit fine time-stamping counter. Each pixel can be programmed to work on one of three different modes: event counting & Integral time-over-threshold (ToT), Only time-over-amplitude (ToA), and ToA & ToT. In order to avoid distributing a very high-speed clock signal into the pixel-array and to save the pixel area, eight pixels (called super pixel) share a high-speed voltage control oscillator (VCO) that is based on a small area RC ring-oscillator. A PLL circuit with an embedded replica of the ring-oscillator is located in the periphery of the chip. By distributing the control voltage to the pixel-array, all pixel-level ring-oscillators are forced to oscillate at 640 MHz. This approach allows us to stabilize the oscillation frequency by an external PLL, and hence to reduce the effect of fluctuations with respect to process parameter variations and temperature changes.

In August of 2011, a prototype called GOSSIPO4 has been designed and fabricated for verification of the basic Timepix3 functionality. It includes a super pixel sharing one fast oscillator with a PLL control. The functionality of the PLL has been verified on this chip. The same PLL structure has been implemented in Timepix3, which was submitted in May of 2013. The architecture and test results of the PLL will be discussed in this paper.
The oscillator control voltage is generated by means of a PLL and will be broadcasted across the super-pixel matrix of a fully-fletched pixel chip for adjustment of the oscillation frequencies, as shown in figure 1. This approach allows to compensate in all pixels for frequency fluctuations caused by both, process parameter variations and temperature changes, with a single PLL in the chip periphery [4].

The developed PLL is based on the work presented in [5]. The loop is composed of a phase-frequency detector, a charge pump, a loop filter, a copy of the RC-controlled oscillator which is instantiated in the super-pixel and a clock divider. The functional blocks are described in some detail in the following.

2.1 Phase frequency detector

The phase-frequency detector uses a tri-state logic block (see figure 2). The \textit{up} and \textit{down} signals controls the charge pump. Two D-flip-flops with D = 1 are triggered by two clock signals which are compared. Ideally, the three states are UP, DN and high impedance. If the reference clock leads the feedback clock, the UP state is generated (the \textit{up} signal remains a logical one) while DN state is produced for the opposite condition. The filter is in high impedance state at steady state. In order to avoid the dead-zone around zero-phase error leading to increased noise, the forth state where the \textit{up} and \textit{down} pulses are “high” simultaneously is enlarged by inserting a delay in the reset path. This ensures that the switches in the charge pump could be opened even if a tiny phase error exists between the reference clock (clk\textit{ref}) and the feedback clock (clk\textit{fb}). The delay time $\tau_1$ has been optimized in order to minimize the dead zone and to limit the perturbation on the control voltage in the steady state of the PLL.
Figure 2. Schematic of the phase-frequency detector. The $\text{ref}_{\text{fast}}$ and $\text{fb}_{\text{fast}}$ signals are available off-chip for monitoring purposes.

Figure 3. Schematic of the charge-pump and the loop-filter.

The output of the other two D-flip-flops ($\text{ref}_{\text{fast}}$ and $\text{fb}_{\text{fast}}$) track the $\text{up}$- and the $\text{down}$-signals with a delay $\tau_2$, hence, realizing a lock-detection circuit whose output is made available off-chip. The value of the delay time $\tau_2$ determines the sensitivity of the loss of lock detection, it has to be chosen relatively large with respect to $\tau_1$ in order to give an accurate representation of the lock status.

2.2 Charge-pump

The charge pump uses a differential architecture with a dummy branch (see figure 3). The two switched current sources charge or discharge the capacitor $C_1$ of the loop-filter, thus, converting the phase and frequency differences into a control-voltage. The branches are controlled by the $\text{up}$- and $\text{down}$-, the $\text{up}$- and $\text{down}$-signals, respectively. The transistors (M5, M6 and M8) form current mirrors providing the biasing current for the charge pump. For charge-sharing minimization, the switch transistors (M1-M4) in the charge pump are minimum size.
2.3 Loop-filter

As discussed in [5], the third-order loop-filter shown in figure 3 eliminates undesired high frequency noise signals and, therefore, ensures a stable control voltage. It consists of two resistors ($R_1$ and $R_2$) and three capacitors ($C_1$, $C_2$ and $C_3$) that create a three-pole one-zero network. To stabilize the system, by adding a resistor $R_1$ in series with the loop filter capacitor $C_2$ introduces a zero in the loop gain. Even in the locked condition, the mismatches between the current of the charge pump and the charge injection of the switch transistors introduce voltage jumps in $U_{ctrl}$. To relax this issue, a second capacitor $C_1$ is added in parallel with $R_1$ and $C_2$. The third branch of the loop filter ($C_3$ and $R_2$) forms another non-dominant frequency pole that further filters high frequency noise on the control voltage $U_{ctrl}$. This loop is of three order, yielding a four-order PLL and improving its stability.

2.4 Frequency-divider

The frequency divider is made of a chain of four D-flip-flops dividing the oscillator output frequency of 640 MHz by 16, hence, yielding the needed 40 MHz feedback-clock.

For measurements on the PLL- and the TDC-performance, the chip was bonded to a standard chip package and mounted on a printed circuit board, as shown in figure 4. The logic stimuli needed for operation as well as the readout of the data are provided by a Spartan-3 FPGA hosted on the multipurpose S3-MultiIO-board developed at the University of Bonn.

3 PLL performance

For the measurements on the PLL performance, the 40 MHz reference clock is provided by an Agilent 81134A signal generator. The outputs of the on-chip LVDS driver are directly connected to a differential probe of a Tektronix MS-O70804 oscilloscope (25 GS/s, 8 GHz bandwidth). The S3-MultiIO-board is used only as power supply.

The Time Interval Error (TIE) defines how far each active edge of the output clock varies from its ideal position. A jitter histogram for a TIE measurement is shown in figure 5. Fitting by a Gaussian distribution yields a width ($\sigma$) of only 23.4 ps.

Figure 6 shows an eye diagram of the 320 MHz output clock. Besides the central branch, two side-branches caused by cross-talk from the positive and the negative edge of the reference clock.
are observed in this plot. This is no issue of the PLL itself, but only of the present test-chip on which the reference-clock and the LVDS-wire-bond pads are located next to each other. The total eye-opening is 1.37 ns on the time axis and about 340 mV on the voltage axis. The main PLL characteristics are listed in table 1.

4 Conclusion

In August of 2011, a prototype called GOSSIPO4 has been designed and fabricated for verification of the basic Timepix3. It includes eight-pixel structures (i.e. super pixel) sharing one fast oscillator with a PLL control. The functionality of the PLL has been verified on this chip. The PLL generates a clock frequency of 640 MHz with a power consumption of 5 mW, at a supply voltage of 1.5 V. Measurements have shown the TIE jitter performance to be below 24 ps RMS at an additional 320 MHz output. The same PLL structure has been implemented in Timepix3, which was submitted in May of 2013. Similar results of the PLL have been observed for Timepix3 [6].

Figure 5. TIE at the 320 MHz output.

Figure 6. Eye diagram of the output frequency of 320 MHz.
Table 1. PLL characteristics.

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>total PLL area</td>
<td>$208 \mu m \times 106 \mu m$</td>
</tr>
<tr>
<td>jitter performance (TIE)</td>
<td>23.4 ps at 320 MHz output</td>
</tr>
<tr>
<td>cycle-to-cycle jitter</td>
<td>50.4 ps at 320 MHz output</td>
</tr>
<tr>
<td>period jitter</td>
<td>31.2 ps at 320 MHz output</td>
</tr>
<tr>
<td>duty cycle</td>
<td>50.75%</td>
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<tr>
<td>power consumption</td>
<td>$\approx 4$ mW</td>
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<tr>
<td>time to lock</td>
<td>4 $\mu$s</td>
</tr>
<tr>
<td>VCO output frequency range</td>
<td>490–740 MHz</td>
</tr>
</tbody>
</table>

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References


