Conference Contribution

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09 June 2012

The research leading to these results has received funding from the European Commission under the FP7 Research Infrastructures project AIDA, grant agreement no. 262025.

This work is part of AIDA Work Package 8: **Improvement and equipment of irradiation and test beam lines.**

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Development of the Data Acquisition System of a Large TPC for the ILC

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Abstract—In this note we report on the developments of the data acquisition (DAQ) system for a large Time Projection Chamber (TPC). A large TPC is proposed as part of the tracking system for an experiment at the future electron positron linear collider ILC. The DAQ system used for large TPC prototypes was initially based on the ALICE DAQ system. This system was successfully used during a series of test beams in DESY with a large TPC prototype. The collaboration is now developing the DAQ system using the most recent technologies to investigate possible architectures for the future experiment.

I. INTRODUCTION

A large Time Projection Chamber (TPC) is proposed as part of the tracking system for a detector at the future electron positron linear collider ILC [1]. The Linear Collider TPC (LCTPC) Collaboration is currently studying a large TPC prototype (60 cm long, with an outer radius of 77 cm), offering some modularity to investigate various gas amplification systems (GEM or Micromegas), pad sizes and geometries as well as different read-out systems. This prototype has already been extensively and successfully tested during more than 10 weeks, with 6 GeV electron beams, in DESY.

The readout electronics of the ILC large TPC prototype is based on the ALICE [2] ALTRO [3,4] ADC chip in combination with a newly developed charge pre-amplifier, PCA16, which is programmable with respect to shaping time, gain, decay time and polarity. The preamplifier was specially developed as a first step towards the final electronics for the ILC TPC. The data acquisition system of the prototype is also based on the ALICE data acquisition system, using the Detector Data Link (DDL) and the PCI Detector Read Out Receiver Card (DRORC) both developed by the ALICE Collaboration.

For the use of the TPC at the ILC, the current readout and data acquisition systems have to be upgraded in different aspects: size of the front-end electronics, power-pulsing

capability, improved digital signal processing and higher bandwidth communication technology for the data acquisition. In this note we will mainly report on the latest developments concerning the front-end electronics and the new data acquisition system: we will report on the status of the design of the new Multi-Chip-Module (MCM) board that can house up to 8 new sALTRO16 chips as well as on the development of a first micro-TCA Advanced Mezzanine Card (AMC) prototype to replace the DRORC.

II. CURRENT DAQ SYSTEM

The current DAQ system used by the LCTPC Collaboration is shown on Fig. 1. The Front End Cards (FEC) contain 8 newly developed PCA16 preamplifier-shaper chip and 8 ALTRO ASICs which perform the AD-conversion. The ALTRO digitizes the analog waveform from the PCA16 in a sequence of 1000, 10 bit samples which are stored in the ALTRO until readout. The sampling frequency can be chosen to be 5, 10 or 20 MHz with full voltage resolution. The PCA16 charge amplifier has been designed with several remotely programmable features like the input signal polarity, the peaking time (between 30 and 120 ns), the gain (between 12 and 27 mV/fC), etc. The programmability of the PCA16 provides a general purpose DAQ system by which many different readout technologies can be tested.

Fig. 1. Current DAQ system used for the LCTPC large TPC prototype.

The FEC are connected to the TPC anode pads through 25 cm long flat Kapton cables. The FECs are placed on a backplane together with a Readout Control Unit (RCU) which controls the readout: data is sent through the 200 MB/s

Manuscript received June 11, 2012. This work is supported by the Commission of the European Communities under the 7th Framework Program and by the Swedish Council (VR). G. De Lentdecker is Research Associate of the Belgian FRS-FNRS.

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Detector Data optical Link (DDL) to the Detector Data Read Out Card (DRORC) a PCI board located in the DAQ PC.

III. A NEW ASIC, THE SALTRO16 AND THE MULTI CHIP MODULE (MCM)

The TPC being conceived for future experiments at the international linear collider aims at detector pads as small as 4 mm^2 and a total material budget as low as 15% radiation length. For example, the ALTRO based readout system for the ALICE TPC at the LHC, allows a maximum packing density that corresponds to 30 mm^2 sized detector pads. Such a density could be achieved by placing the electronics on dedicated read-out boards mounted perpendicularly to the detector end-plate. Each board accommodates 128 channels and consumes a power of 50 mW/channel, which has in turn to be dissipated by a large water cooling system. This leads to a significant amount of real estate and can only be achieved with a material budget of 500% radiation-length. This architecture was the base of the DAQ system used for the test beams of the large TPC prototype (see section II).

The close integration of both analogue and digital circuits, ultimately in a single chip, constituted therefore an important step, aiming at a highly optimized circuit in terms of density and low-power. That is the essence of the sALTRO16 chip. A small number of chips have been delivered to CERN where it was checked that they meet the specifications.

Fig. 2. (left) Layout of one side of the Multi Chip Module (MCM). (right) Schematic drawing of one readout module equipped with 25 MCM.

The original plan was to mount the electronics directly onto the TPC pad plane using bump bonding to minimize the size requirement. However, the replacement of a malfunctioning chip is a difficult operation which will require advanced equipment and that the module be dismounted from the TPC endplate. Therefore the dies will be mounted on small carrier boards ($8.9 \times 12 \text{ mm}^2$). Four of these carrier boards are mounted on each side of a larger board, the Multi Chip Module (MCM) as shown on Fig. 2 (left). One MCM ($25 \times 32.50 \text{ mm}^2$) will contain $8 \times 16 = 128$ channels, like the current FEC. One detector module would be equipped with 25 MCMs, that is 3200 pads of $1.1 \times 8.4 \text{ mm}^2$, as shown on Fig. 2 (right). The MCM will be directly connected to a Board Controller (BC) equipped with a Spartan6 FPGA, on top of the MCM in the so-called horizontal layout as shown on Fig. 3.

Fig. 3. Two views of the MCM + BC mounted on top of the pad plane. The grey chip on the top represent the FPGA and the dark green rectangles, the sALTRO16 chips.

IV. DATA READOUT

The data readout is being investigated. An attractive option is to send the data from the BC to the new Scalable Readout Unit (SRU) shown in Fig. 4. The SRU is developed within the RD51 Collaboration [5] and could be adopted by ALICE EMCAL for the ALTRO bus readout. For the LCTPC large prototype readout, one SRU could replace up to two sets of RCU, DCS and SIU to read 4 GTL bus. With the SRU, the serial readout of 10 FECs /GTL bus will be replaced by the parallel readout of 40 FECs. The SRU has 40 RJ45 inputs to connect to the FECs and can communicate to the DAQ DRORC like the current RCU. The data will then be sent off the detector area through the 200 MB/s Detector Data optical Link (DDL). The SRU can also communicate via Gigabit Ethernet. Finally note that the SRU could also be used with the current FECs, through a small adaptor card.

Fig. 4. The Scalable Readout Unit (SRU) designed by the RD51 Collaboration [5] as a candidate for the readout of the LCTPC large prototype.

In the current system the data are sent through the Detector Data optical Link (DDL) to the Detector Data Read Out Card (DRORC), a PCI board located in the DAQ PC. For the future DAQ we propose to develop an Advanced Mezzanine Board (AMC) host in a μ TCA crate. The AMC would be equipped with a powerful FPGA (a Virtex 6 is now under

consideration). The AMC would use the PCIe protocol to communicate with μ TCA backplane where the bandwidth could reach up to 4x4Gb/s.

Fig. 5. Block diagram of the future DRORC AMC Board.

Being our first μ TCA experience, a first AMC has been designed without FPGA. It is however designed such that an FPGA could easily be added through a small mezzanine board. This first AMC contains several DC-DC converters, a LDO regulator, one MMC (Module Management Controller) and one SFP cage. This board has been designed mainly to gain experience with the μ TCA standard and as a testbed to study the ramp up time and noise measurement of the DC-DC converters, to check the voltage stability after a very low noise LDO (mandatory for high speed communication controllers), MMC configuration as well as remote FPGA reconfiguration, etc.

Fig. 6. Our first AMC prototype, without FPGA.

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V. CONCLUSIONS

In this note we summarize the developments of the DAQ system for a large TPC planned to be used as the central tracker for an experiment at a future linear collider. Initially based on the ALICE readout electronics, the new DAQ includes the new sALTRO16 chip, a new design of the FEC board (MCM+BC), the use of the SRU instead of the RCU, the DDL link, and a new DRORC based on the μ TCA standard.