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Radiation tolerance of an SLVS receiver based on commercial components

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\textbf{ABSTRACT}: The capability of ProASIC3L FPGAs to receive SLVS signals has been studied in laboratory conditions and after irradiation. The irradiation has been performed using a Cs-137 source. The SLVS communication has remained functional after 201 Gy. The slowest rise time after irradiation is 324 ps, negligibly degraded with respect to the pre-irradiation rise time.

\textbf{KEYWORDS}: Radiation damage to electronic components; Front-end electronics for detector read-out; Digital electronic circuits

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1 Introduction

High energy physics experiments are constantly trying to acquire bigger amount of data while limiting the power consumption. The Low-voltage differential signaling standard (LVDS) has been used extensively for this purpose. SLVS is a newer standard signaling protocol conceptually similar to LVDS, but with lower common-mode and differential-mode voltages, which makes it especially suitable when high speed and low power are required. It is gaining some popularity in data acquisition systems for high energy physics experiments [1], where systems are also exposed to a mixture of radiation including gamma rays, electrons, neutrons and charged hadrons. Although SLVS has been standardized in 2001, it is still difficult to find commercial electronic components capable to translate SLVS to or from other protocols. No study is known to the authors about the radiation tolerance of SLVS commercial components. In this article we present our first results in this respect.

1.1 Component selection

SLVS has a nominal VOL of 0 V (ground) and a nominal VOH of 400 mV [2]. This implies a common mode of 200 mV and a differential voltage of 400 mV. The flash-based FPGA family ProASIC3L [3] (A3PL, built on a 0.13-um CMOS process) nominally supports LVDS but does not support SLVS. According to the table 2-174 of the ProASIC3L Data Sheet [3], the electrical characteristics of the LVDS input buffers are:

<table>
<thead>
<tr>
<th>Input Common Mode Voltage Min</th>
<th>50 mV</th>
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<tbody>
<tr>
<td>Input Differential Voltage Min</td>
<td>100 mV</td>
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</table>

Based on these electrical characteristics, we hoped that the ProASIC3L LVDS input buffers would be compatible also with SLVS signals. We have in fact verified that this is the case.
2 Electrical tests

Electrical tests in a normal lab environment were performed to verify the capability to receive SLVS signals. We have used the Cortex-M1 ProASIC3L Development Board (Part Number M1A3PL-DEV-KIT sold by Actel) together with the SLVS test card shown in figure 1. This card has a socket U1 with an LVDS-SLVS translator ASIC (CRT758) developed by CERN and described on section IV.C of reference [1].

The concept of the test is to generate a signal in the FPGA, send it out as LVDS to the translator (and send out a copy as CMOS to an oscilloscope), then the translator converts it to an SLVS signal which is sent back to the FPGA. The FPGA receives it with an LVDS input buffer, then the resulting signal is sent out as a CMOS level to an oscilloscope, for comparison. Figure 2 shows a block diagram of the test apparatus.

The 3-resistor network near OUTBUF_LVDS is required for proper behaviour of OUTBUF_LVDS, as described on reference [3]. No particular effort has been done to minimize the electrical noise of the apparatus, as shown on photography on figure 3. The LVDS signal is transmitted over two coaxial cables into two SMA connectors; the shields of the coaxial cables are connected to the ground of the Actel board. The SLVS signal is transmitted over two unshielded wires into a header connector on the Actel board. The two active probes are connected to tx_CMOS and rx_CMOS.

We have created an Actel project following the scheme in figure 2. The FPGA doubles the frequency of the 48 MHz clock signal with one of its PLL and generates an internal 96 MHz clock (period of \(\sim 10.4\) ns), used to generate synchronous signals. Based on the position of the on-board switch, the FPGA can generate different signals.

With an appropriate setting, we generated a clock-like signal, which is shown on the yellow trace on figure 4. The blue trace on the same figure shows that the FPGA is able to receive correctly this SLVS signal. In general, proper reception of a clock-like digital signal (DC-balanced) does not guarantee that all digital signals of similar frequency will be received correctly. In order to verify that the FPGA is capable to receive SLVS signals of arbitrary shapes, we generated a signal with a positive pulse of about 10.4 ns followed by about 156 ns (15 cycles of the 96 MHz clock) where the signal remains low. This signal is not DC-balanced and for example, it emulates applications with fast synchronous commands. The generated signal is shown on the yellow trace of figure 5. The same figure shows that the corresponding received signal (blue trace) is received properly. We can conclude that the capability of the FPGA to receive SLVS signals does not depend on the signal shape (up to a data rate of at least 48 MHz).

The SLVS test board has a 4-bit switch (J4 in figure 1) which allows modulating the SLVS output current between 0.5 mA and 2 mA. The ProASIC3L FPGA receives correctly the SLVS signal for all values of the current in this range. Note that the termination on the Actel board is 100 \(\Omega\), thus setting the current of the SLVS test board output to 2 mA generates a voltage swing of 200 mV per wire, which corresponds to the standard SLVS levels. If we set the current of the same output to 0.5 mA, we generate a swing of only 50 mV per wire, which is very small compared to other digital signalling standards, but the FPGA is still able to receive it. This is not totally surprising because it corresponds to an input differential voltage of 100 mV, which matches the low end of the LVDS characteristics declared in the ProASIC3L Data Sheet [3].
Figure 1. SLVS test board (Courtesy of INFN Torino) modified for the purpose of the test, in order to act as a LVDS-to-SLVS translator.
Figure 2. Apparatus for the electrical test. The oscilloscope is used with single-end active probes.

Figure 3. Apparatus of the electrical tests, the LVDS/SLVS translator chip is on a socket on the left side.

The electrical tests show that the ProASIC3L FPGA is able to receive an arbitrary 48 MHz SLVS signal using any of its integrated LVDS input buffers. The test setup described here is not suitable for fine measurements of jitter and noise margins.

3 Irradiation tests

Having verified that ProASIC3L FPGAs can receive SLVS signals in a normal lab environment, we have tested the same capability in a radiation environment. In general, in order to characterize the
Figure 4. 48 MHz signals at the beginning and at the end of the chain.

Figure 5. A non DC-balanced signal at the beginning and at the end of the chain.
radiation tolerance of a device, the tests must assess its tolerance to the total ionizing dose (TID) and to single event effects (single even upset, single event latchup, single event burnout, etc.) Testing the radiation tolerance of an FPGA is often more complex than testing other devices, because the behaviour typically depends on the program loaded into the FPGA and depends on which features of the FPGA are enabled by the program. Previous irradiation tests of the ProASIC3L FPGA [6] have been fairly exhaustive with regards to the features declared in its Data Sheet. No tests have been published regarding its SLVS abilities (this is not surprising as these capabilities are outside the specifications of the FPGA).

In the particular case of testing the radiation tolerance of the ability to receive SLVS signals, we do not need to test the single event latchup and single event burnout, because the previous tests remain valid independently from the electrical inputs applied to the FPGA. We do not even need to test single even upset because this is a concern for memory elements, which is not the case of the circuitry used to receive SLVS. A test apparatus different from what described in the previous sections has been prepared. The Device Under Test (DUT) is a A3P250L FPGA from the same ProASIC3L family of Microsemi. The FPGA has been programmed with a simple design which has four LVDS inputs connected to four LVDS outputs, without any logic or memory element in between.

The irradiation facility used is the Gamma Irradiation Facility, a Cs-137 source at CERN [4]. During the irradiation the DUT always remained powered up; one of the input was constantly fed with a toggling SLVS signal generated by the card on figure 1 via a 3-meter CAT6 network cable; two of the inputs were fed with toggling LVDS signals (via the same network cable) and the forth input was left unconnected. With this apparatus mounted on the Gamma Irradiation Facility, we have periodically stopped the irradiation and we have monitored the activity on the outputs. In order to measure the TID absorbed by the DUT, we have used dosimetric films of the same type described on section III.B of reference [5]. The strips were mounted on the side of the DUT away from the source (so the DUT was between the source and the films).

After a TID of at least 201 Gy, the irradiation facility was stopped for a major maintenance operation, while the DUT appeared to be normally functional. A TID of 201 Gy is lower than what was initially planned, but it is higher than the TID experienced by the electronics of various particle detectors, for instance the Hadronic Calorimeter of the CMS experiment [7], the calorimeters of the LHCb experiment [8], and most detectors in electron-positron colliders (see for instance reference [9]). So it was decided to remove the DUT from the radioactive environment and measure its ability to receive SLVS. We have connected the SLVS driver via the same 3-meter cable used during the irradiation sequentially to the four LVDS inputs of the DUT, and we have measured the rise time at the four corresponding outputs. The SLVS signal after the 3-meter cable appeared to have a reduced swing of about 100 mV, as shown on figure 6. This is the signal seen as an input of the DUT during irradiation and during the measurements; its rise time has been measured as on table 1.

The measurements on the four DUT LVDS outputs are reported on table 2. The four outputs are nominally identical; they are color-coded for the simple purpose of identifying them. They show that after irradiation the DUT is still able to receive correctly an SLVS signal significantly smaller than a typical signal.
Figure 6. SLVS signal acquired at the receiving end of the cable, with a 1.5 GHz differential probe P6248 and the oscilloscope TDS7254.

Table 1. Rise time of the SLVS signal at the receiving end of the cable (as seen by the FPGA inputs).

| Measurements of the input signal rise-time [20% – 80% in ps] | 238 | 263 | 261 | 284 | 286 | Average = 266.4 |

Table 2. Rise time of the LVDS signals sent out by the DUT, when the DUT is fed with the SLVS signal shown above.

<table>
<thead>
<tr>
<th>Measures of rise time [20% – 80% in ps] at the DUT outputs</th>
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<tbody>
<tr>
<td>CHANNEL</td>
</tr>
<tr>
<td>Green</td>
</tr>
<tr>
<td>Blue</td>
</tr>
<tr>
<td>Brown</td>
</tr>
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4 Conclusions

The tests performed show that the ProASIC3L FPGAs are able to receive SLVS signals of a reduced swing of 100 mV after a total ionizing dose of at least 201 Gy. The degradation in the rise time is modest if at all existing, the slowest rise time after irradiation is 324 ps.
References


