Level-1 Data Driver Card of the ATLAS New Small Wheel Upgrade

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On behalf of the ATLAS Muon Collaboration

MOCAST, 14-15 MAY 2015, Athens

15/05/2015
Overview

• CERN & ATLAS experiment
• NSW electronics
• L1DDC
  • General description
  • Connectivity
  • Rates
  • Components
  • Placement
• L1DDC prototype 1 & 2
• Summary
CERN & ATLAS experiment

- CERN – largest particle physics laboratory (Franco-Swiss borders near Geneva)
- Large Hadron Collider - largest and most powerful particle accelerator
- 27Km ring, 100m under surface
- 4 experiments (ALICE, ATLAS, CMS, LHCB)
The ATLAS experiment

- ATLAS - General purpose detector
- Small Wheels are located between end-cap calorimeter and end-cap toroid
- Consist of CSC, TGC, MDT detectors
- 10 m in diameter
- High background rate - $L = 2\times10^{34}\text{cm}^{-2}\text{s}^{-1}$ during LHC Run-3 and HL-LHC
- Particle rate will be increased
New Small Wheel

- NSW is a set of precision tracking and trigger detectors able to work at high rates
- 2 technologies: sTGCs and micromegas detectors will provide tracking and trigger data
- 8 small + 8 large sectors per wheel
- 8 sTGCs + 8 micromegas planes per sector
NSW electronics trigger and dataflow

On-detector

sTGC - On NSW rim
- pad trigger
- router

strip TDS

1/FEB

VMM
- MM
- ROC
- SCA

Front end board

# of VMMs per FEB:
- MM: 8
- sTGC: strips 5, 6 or 7
- sTGC pad 2 or 1
- sTGC wire 1

Off-detector

USA15
- Trigger processor
- Trigger processor

From Big Wheel

Sector logic

Trigger monitor

network

FELIX
- TTC

calibration

Event monitor

ROD

Config

DCS

E-links

Bidirectional fiber

One way fiber

Twinax cable

Twinax cable
L1DDC connectivity

• 3 distinct paths to the front ends through one bidirectional link

• DAQ data
  - Level-1 data (Time, charge and strip address)
  - Configuration data

• ASICS
  - GBTX
  - GigaBit TransImpedance Amplifier (GBTIA) – Photo Diode
  - GigaBit Laser Diode (GBLD) - Laser

• Line rate 4.8Gbps

• 1 frame of 120bits @ 40MHz (25ns)
  - Header 4 bits
  - Slow control 4 bits
  - Data 80 bits
  - FEC 32bits (2 interleaved Reed-Solomon encoding)

• Error correction and error detection
  - Up to 16 consecutive corrupted bits can be corrected

• User bandwidth 3.36Gbps
**GBTX ASIC Connectivity**

- 1 e-link has 3 differential pairs: Clock, Data out, Data in
- Up to 40 front-ends can be connected to 1 GBTx combined in 5 banks
- Each bank can support (programmable rate)
  - 8 front ends @ 80Mbps
  - 4 front ends @ 160Mbps
  - 2 front ends @ 320Mbps
- Each bank can be configured at different rate
- 1 L1DDC is connected to 8 micromegas FEs
  - 1 cable for FE to L1DDC connection
    - 1 e-link for the ROC
    - 1 e-link for the SCA
- 1 L1DDC is connected to 3 sTGC FEs
  - 1 cable for FE to L1DDC connection
    - 3 e-links for the ROC
    - 1 e-link for the SCA
- Slow Control channel @ 80Mbps dedicated to ADDC (1 e-link)
- E-links use Scalable Low-Voltage Signaling (SLVS), $V_{cm} = 0.2V$, swing 200mV
L1DDC connectivity with the MMFE8 and ADDC boards

- SCA ASIC will be added to the ADDC board
  - Slow Control channel of the GBTX will be used for the configuration of the SCA.
- 2 extra differential pairs (clocks) will be send from the L1DDC to the ADDC
  - Either from the 8 programmable clocks of GBTX.
  - Either form the two spares of the bank1.
L1DDC

• Different designs
  - Micromegas
    • 9 mini SAS connectors (8 for FEs, 1 for ADDC)
  - sTGC
    • 3 mini SAS connectors (3 for FEs)

• Voltage levels
  - 2.5V Digital (VTRX)
  - 1.5V Analog (GBTX)
  - 1.5V Digital (GBTX)

• Components
  - GBTx ASIC, VTRX optical transceiver, 2 x FEAST DC-DC converter
  - Power connector - Molex 0015912025

• Power consumption
  - 3.5Watts (estimated)
L1DDC components

- **GBTX ASIC**
  - BGA 400pins package
  - Pitch 0.8mm
  - Radiation hard ASIC - IBM 130nm technology
  - Power supply 1.5V
  - Power consumption 2.2Watts

- **VTRX optical transceiver**
  - GBTIA
    - 2.5V @ 0.05Amps
    - Power consumption 0.12Watts
    - Bit rate 5Gb/s
    - 0.13-μm IBM CMOS8RF-LM technology
  - GBLD
    - 2.5V @ 0.2Amps
    - Power consumption 0.5Watts
    - Bit rate 5Gb/s

- **FEAST DC-DC converter**
  - Input voltage from 5V to 11.5V, 4A load capacity
  - 76% efficiency
  - It contains a radiation tolerant ASIC with total ionizing dose up to 200Mrad (Si) and displacement damage up to 5 x 10^{14} n/cm2
L1DDC placement

- L1DDC will be placed radially on both sides of micromegas and sTGC detectors
- 1 L1DDC will serve the 8 front ends of the one side of each plane
- For the micromegas L1DDC will be placed on the center to minimize the cable length (fixed length @ 3 m)
- Elastic thermal foam will be used for better connectivity to the cooling channel
L1DDC - Prototype 1 & 2

• Prototype 1
  • Already fabricated
  • Size 210mm x 144mm
  • Layers used : 14
  • Alternative paths in case of GBTX failure
  • Input voltage 3.6V - 42V
  • GBTx, GBTIA & GBLD (VTRX) ASICs
  • Xilinx FPGA Artix7 - xc7a200t-3FBG484
  • SFP+, Gigabit Ethernet, VTRX, miniSAS 36p, SMAs
  • Still in debugging process
  • Board is functional
  • No radiation tolerant board

• Prototype 2
  • Design in progress (same as final board)
  • Size 200mm X 50mm
  • 12 Layers will be used
  • Input voltage 5V - 12V
  • Use only radiation hard components (GBTx, VTRX, FEAST)
  • Can be tested in radiation and magnetic fields
  • Estimate final power consumption

Top side of L1DDC prototype-1 board
Summary

• L1DDC collects the Level-1 Data and distributes the TTC data to the front end and ADDC boards
• L1DDC is a fully radiation tolerant board
• Fulfills all ATLAS NSW upgrade requirements
• Fully compliant with LHC rates
• Has SEU mechanisms to assure signal integrity
• Different L1DDC boards will be fabricated for micromegas and sTGCs detectors
Thank you

Questions
### MMs and sTGC rates

- MMs rates exceed maximum of e-link rate.
- 2 elinks/MMFE8 will be used for the inner portions (1 elink @ 320Mbps + 1 elink@160 Mbps = 480Mbps).
- 3 sTGC FEs will be connected to 1 L1DDC (1 twinax cable and 10 differential pairs)

#### Table

<table>
<thead>
<tr>
<th>sTGC FE</th>
<th>Rate (Mbps)</th>
<th>Bank channel</th>
</tr>
</thead>
<tbody>
<tr>
<td>Small</td>
<td>Large</td>
<td>E-link</td>
</tr>
<tr>
<td>Wire D3</td>
<td>25.6 41.8</td>
<td>Strip D3</td>
</tr>
<tr>
<td>Wire D2</td>
<td>47.0 66.5</td>
<td>Strip D2</td>
</tr>
<tr>
<td>Pad D2</td>
<td>49.5 72.2</td>
<td>Strip D2</td>
</tr>
</tbody>
</table>

#### Diagram

![sTGC twinax for FE board readout to L1DDC-sTGC](image)
L1DDC prototype1 - technical characteristics

• **FPGA Artix 7 (xc7a200t-3fbg484)**
  • Configures the GBTx
  • Implements the I2C protocol for the communication with the configuration registers
  • Reads and sends the data in case of GBTx failure

• **Inputs & outputs**
  - Detector side
    • Elinks (LVDS or SLVS differential)
  - Counting room side
    • VTRX optical tranceiver
    • 10/100/1000 ethernet
    • SFP
    • SMA

• **JTAG port**

• **SMA & RJ45 for reference clock and trigger**
L1DDC prototype1 - technical characteristics

• **Voltages Levels**
  - 1.5V Digital (GBTx)
  - 1.5V Analog (GBTx)
  - 2.5V Digital (VTRx, FPGA) Direct from LTM4619
  - 3.3V Digital (efuses, SN65LVDT122) Direct from LTM4619
  - 1.2V Analog MGTA\textsubscript{VTT} (FPGA)
  - 1.0V Analog MGTA\textsubscript{VCC} (FPGA)
  - 1.0V Digital VCC\textsubscript{INT}, VCC\textsubscript{BRAM} (FPGA)
  - 1.8V Digital VCCAUX (FPGA)

• **4 LT8612 DC-DC Converters**
  - Single 6A output

• **Use of 6 ADP1755 LDOs to step down the voltage**
  - Single output @ 1.2A

• **Anything to LVDS translators (SN65LVDT122)**
  • Convert GBTx output (SLVS) to LVDS standard
### PCB Stack Up

<table>
<thead>
<tr>
<th>Layer</th>
<th>Type</th>
<th>Thickness (mil)</th>
<th>Single ended</th>
<th>Impedance</th>
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<tbody>
<tr>
<td>Top side solder mask</td>
<td>0.5 mils</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>L1</td>
<td>Top copper + plating</td>
<td>1.4 mils</td>
<td></td>
<td>97.48Ω</td>
</tr>
<tr>
<td></td>
<td>prepreg</td>
<td>4 mils</td>
<td>4/4/4 mils - 100Ω ±/− 10%</td>
<td>97.48Ω</td>
</tr>
<tr>
<td>L2</td>
<td>copper</td>
<td>0.7 mils</td>
<td>4/4/4 mils - 100Ω ±/− 10%</td>
<td>97.48Ω</td>
</tr>
<tr>
<td></td>
<td>core</td>
<td>8 mils</td>
<td>100Ω ±/− 10%</td>
<td>97.48Ω</td>
</tr>
<tr>
<td>L3</td>
<td>copper</td>
<td>0.7 mils</td>
<td>4/4/4 mils - 100Ω ±/− 10%</td>
<td>97.48Ω</td>
</tr>
<tr>
<td></td>
<td>prepreg</td>
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<td>97.24Ω</td>
</tr>
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<td>99.24Ω ±/− 10%</td>
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<td>core</td>
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<td>99.24Ω ±/− 10%</td>
<td>99.24Ω</td>
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<td>99.24Ω ±/− 10%</td>
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<tr>
<td></td>
<td>prepreg</td>
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<td>99.24Ω ±/− 10%</td>
<td>99.24Ω</td>
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<td>99.24Ω ±/− 10%</td>
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</tr>
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<td></td>
<td>core</td>
<td>6 mils</td>
<td>99.24Ω ±/− 10%</td>
<td>99.24Ω</td>
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<tr>
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<td>99.24Ω ±/− 10%</td>
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</tr>
<tr>
<td></td>
<td>prepreg</td>
<td>4 mils</td>
<td>99.24Ω ±/− 10%</td>
<td>99.24Ω</td>
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<tr>
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<td>99.24Ω ±/− 10%</td>
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<tr>
<td></td>
<td>core</td>
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<td>99.24Ω</td>
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<td>99.24Ω ±/− 10%</td>
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<tr>
<td></td>
<td>prepreg</td>
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<td>99.24Ω</td>
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<tr>
<td>L10</td>
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<td>99.24Ω ±/− 10%</td>
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<tr>
<td></td>
<td>core</td>
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<td>99.24Ω ±/− 10%</td>
<td>99.24Ω</td>
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<tr>
<td>L11</td>
<td>copper</td>
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<td>99.24Ω ±/− 10%</td>
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<tr>
<td></td>
<td>prepreg</td>
<td>8 mils</td>
<td>100Ω ±/− 10%</td>
<td>100Ω ±/− 10%</td>
</tr>
<tr>
<td>L12</td>
<td>copper</td>
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<td>99.24Ω ±/− 10%</td>
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<tr>
<td></td>
<td>core</td>
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<td>99.24Ω ±/− 10%</td>
<td>99.24Ω</td>
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<tr>
<td>L13</td>
<td>copper</td>
<td>0.7 mils</td>
<td>99.24Ω ±/− 10%</td>
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<tr>
<td></td>
<td>prepreg</td>
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<tr>
<td>L14</td>
<td>Bottom copper + plating</td>
<td>1.4 mils</td>
<td></td>
<td>97.48Ω</td>
</tr>
<tr>
<td></td>
<td>Bottom side solder mask</td>
<td>0.5 mils</td>
<td></td>
<td>97.48Ω</td>
</tr>
</tbody>
</table>

| TOTAL | | | 90.2 mils | 2.291 mm |
L1DDC functionality

Front End board connections – 8 FEB/L1DDC

ART

- mSAS 26p
- mSAS 26p
- mSAS 26p
- mSAS 26p
- mSAS 26p
- mSAS 26p
- mSAS 26p
- mSAS 26p

sma: Trigger

RJ45

- Trigger and time

power

SFP+

Artix-7

GBTx

- SMA: GBTx reference clock

programmable clock output (8 clocks)

15/5/2015

MOCAST 2015
2 alternative paths to read and send the data
• From FPGA in case of failure of GBTx
• Directly from GBTx

**CBTL04083A** PCI Express Gen3 switch up to 8.3Gb/s
• Low intra-pair skew: 5 ps typical
• Low inter-pair skew: 35 ps maximum
Connectivity: MMFE8 – L1DDC – ADDC
Twinax cables

- 3M mini SAS cables
- 36p positions
- 8 differential pairs + 8 sidebands
- Part No: 8F36-AAA105