A Fast hardware tracker for the ATLAS Trigger

Carlo Pandini\textsuperscript{a,*}, on behalf of the ATLAS Collaboration

\textsuperscript{a}LPNHE, Paris, France

Abstract

The trigger system at the ATLAS experiment is designed to lower the event rate occurring from the nominal bunch crossing rate of 40 MHz to about 1 kHz for a LHC luminosity of the order of $10^{34}$ cm$^{-2}$ s$^{-1}$. To achieve high background rejection while maintaining good efficiency for interesting physics signals, sophisticated algorithms are needed which require extensive use of tracking information. The Fast TracKer (FTK) trigger system, part of the ATLAS trigger upgrade program, is a highly parallel hardware device designed to perform track-finding at 100 kHz. Modern, powerful Field Programmable Gate Arrays (FPGA) form an important part of the system architecture, and the combinatorial problem of pattern recognition is solved by 8000 standard-cell ASICs used to implement an Associative Memory architecture. The availability of the tracking and subsequent vertex information is an important part of the system architecture, and the combinatorial problem of pattern recognition is solved by 8000 standard-cell ASICs used to implement an Associative Memory architecture. The availability of the tracking and subsequent vertex information within a short latency ensures robust selections and allows improved trigger performance for the most difficult signatures, such as $b$-jets and $\tau$ leptons.

Keywords: FastTracker, FPGA, Associative Memory, LHC Run-2, ATLAS trigger upgrade

1. Introduction

The ATLAS experiment conducted very successful data taking during the first run of the LHC (Run-1) at a maximum center of mass energy of 8 TeV, up to the end of 2012 \cite{1}. In June 2015 the LHC resumed proton-proton collisions at a higher center of mass energy of 13 TeV. The instantaneous luminosity will reach a maximum of about $1.3x10^{34}$ cm$^{-2}$ s$^{-1}$ in Run-2 (2015-2018), rising to about $2x10^{34}$ cm$^{-2}$ s$^{-1}$ in Run-3 (2020-2022). Following Run-3 the LHC and the experiments will be upgraded for the High Luminosity LHC (HL-LHC) phase. From the Run-1 experience we may learn two important lessons: a new Higgs boson particle has been discovered via its bosonic decay modes and evidence has been observed of fermionic decays to a two $\tau$ final state. In addition to this, no compelling evidence of physics beyond the Standard Model has been observed at the electroweak scale, which seems to imply that either it resides at higher energy scales or it is located in regions hard to probe experimentally. In both cases the final state signatures are challenging to reconstruct and background rates make triggering difficult. The challenge of triggering in Run-2 and forthcoming LHC runs is the main motivation for the addition of a fast hardware tracker (FTK) that provides global track information to the ATLAS Trigger system, increasing its capability to target interesting physics signatures that are hard to disentangle from backgrounds. The ATLAS Trigger consists of two levels: a fast hardware-based trigger at Level-1 with a maximum output rate of 100 kHz and a software-based High Level Trigger (HLT). The main goal of FTK \cite{2} is to provide global track reconstruction from silicon detector hits at the output rate of the Level-1 trigger system, with quality comparable to offline tracking algorithms and in time for the HLT selection.

2. FTK Architecture and System Design

In order to be able to provide fast tracking at the large data rates resulting from full ATLAS Inner Detector (ID) readout at the Level-1 trigger rate, FTK exploits massive parallelization performing track recognition over 64 angular regions ID regions simultaneously. Data collected in the Pixel detector (including the new Insertable B-Layer (IBL)) and SemiConductor Tracker (SCT) of the ID are sent through S-LINK fibers to Data Formatter boards (DF), which take care of the clustering of the ID hits, organize them in 12 logical layers corresponding to the ID barrel and endcap layers and disks, and assign them to the 64 angular regions region. One DF board contains two FPGAs, which are assigned to one angular region region each. The DF transmits the clustered hits to a Data Organizer smart database (DO), which converts them to coarse resolution “super-strips” (SS) that are used for track recognition and stores the full resolution hits. The Associative Memory board (AM) is the heart of the FTK design: it receives coarse resolution hits from the DO and compares them with a bank of pre-computed patterns, built from all the possible combinations of SS in 8 of the 12 logical layers of the ID (4 for the Pixel and 4 for the SCT detectors). The strength of the FTK design is the high parallelism of the AM chip, which allows all the pre-loaded patterns to be compared with the incoming hits almost simultaneously. Patterns with matching hits in at least 7 out of 8 layers are transmitted back to the DO, which retrieves full resolution hits for the SS composing the matching patterns and sends them to the subsequent board, the Track Fitter (TF). In order to speed up the track fitting, the TF stores a set of constants for each detector location performing track recognition over 64 angular regions ID regions simultaneously.
3. Associative Memory Chip and Pattern Matching

The Associative Memory chip is designed as an array of Content Addressable Memory cells (CAM), able to receive a data query and replies if and where data matching the query is located within its own memory. The AM chip receives as input the event hit positions and gives as output all the hit combinations that match a pattern contained in the memory. Patterns stored in the AM consist of blocks of information containing a set of positions in each of the 8 layers along a possible track trajectory and the necessary logic to compare this set with the actual position of each hit in the event. The comparison between incoming data and pre-loaded patterns is performed in parallel, hence the pattern matching can be obtained in one AM chip clock cycle. The latest version of the AM chip is able to store up to 128k patterns. The pattern definition is optimized to respect the hardware limitations while maintaining high matching efficiency. These goals are achieved using variable resolution patterns, which are composed of larger SS (coarse resolution) in layers where we want to maximize the acceptance for tracks corresponding to interesting physics processes, and thinner SS (fine resolution) in layers dominated by electronic noise and backgrounds. This variable resolution functionality combines the advantages of thin patterns (better background rejection and a reduced traffic between the AM chip and the auxiliary boards) and coarse resolution patterns (high matching efficiency and reduced number of patterns stored on the AM chip), and is a very important improvement in the associative memory technology.

4. Physics Performance

The identification of $\tau$ leptons is important for both SM processes, such as the Higgs boson decay, and new physics signatures. The $\tau$ decay channels are dominated by the hadronic mode with a branching ratio of about 65%, which produces a physics signature similar to that of hadronic jets. Hadronic $\tau$ ($\tau_{\text{had}}$) decays are however characterized by the presence of either 1 or 3 charged particle tracks confined in a narrow cone, surrounded by a small amount of QCD radiation. FTK will provide track information at the start of the HLT selection, maximizing the rejection of multijet events while preserving efficiency for $\tau_{\text{had}}$ decays. Figure 1 shows the identification efficiency for a simple HLT selection based on FTK track information for a sample of simulated gluon fusion $H \rightarrow \tau_{\text{had}}\tau_{\text{had}}$ events passing a Level-1 single-$\tau$ trigger requirement [3]. The efficiency is shown in red with respect to the Monte Carlo truth and in blue with respect to the corresponding offline selection, as a function of the $\tau_{\text{had}}$ transverse momentum $p_T$. The same efficiency for a multijet sample is plotted in black, with respect to the offline selection. This comparison shows that it is possible to obtain a large rejection of the multijet background at the HLT using tracking information from FTK. Both simulated datasets correspond to a center of mass energy of $\sqrt{s}=14$ TeV, with an average of 60 pile-up interactions per event.

5. Conclusion

The Fast TraKer system is part of the ATLAS trigger upgrade programme and exploits a high level of parallelism to perform global tracking at the full output rate of the Level-1 system. Tracks reconstructed by FTK can be used to improve the HLT performance for the identification of complex signatures, such as hadronic decays of $\tau$ leptons, b-jets, missing transverse energy or interaction vertices. FTK will start operation for a limited geometrical region of the ID in late 2015 and will be extended to provide full coverage in 2016.

References