A 10 MHz MICRO POWER CMOS FRONT-END FOR DIRECT READOUT OF PIXEL DETECTORS

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Abstract

In the framework of the LAA project for detector R & D, a micropower circuit of $200\text{ }\mu\text{m} \times 200\text{ }\mu\text{m}$ with a current amplifier, a latched comparator and a digital memory element has been tested electrically and operated in connection with linear silicon detector arrays. The experimental Direct ReadOut (DRO) chip comprises a matrix of 9×12 circuit cells and has been manufactured in a $3\text{ }\mu\text{m}$ CMOS technology. Particles and X-ray photons below 22 keV were detected, and thresholds can be set between 2000 and 20000 e^- . The noise is less than 4 keV FWHM or 500 e^- r.m.s. and the power dissipation per pixel element is 30 μW . The chip can be coupled to a detector matrix using bump bonding.

1. INTRODUCTION

At all times elementary particle physics has used tracking detectors, from nuclear emulsions through bubble chambers to time projection chambers, in order to perform multiplicity determination, momentum or lifetime measurement, particle identification, or just to see what happens. In the TeV energy range calorimetry is to play the major role, but the statement that tracking will be unnecessary sounds like a rationalization for the virtual absence of appropriate tracking devices for the TeV hadron collider environment. It can be assumed that, if they exist, good devices will find important applications, and therefore the development of an experimental pixel detector is part of the LAA detector R & D project.

The critical properties for such tracking devices will be: full coverage around the interaction region (hermeticity), low effective mass, granularity adapted to resolve particles in high multiplicity jets, precision in the micron region in 3 dimensions, speed in the range 10-100 MHz, power consumption below 1 kW per m^2 and radiation tolerance in the kGy range. Different groups are conducting research on gas-filled wire chambers and drift chambers, scintillating fiber detectors and semiconductor detectors for use in TeV hadron colliders.

Silicon pixel detectors with true 2-dimensional Direct ReadOut (DRO, as opposed to charge-coupled CCD shifted readout) promise to combine most of the required properties, and their development can be accelerated by drawing on achievements in microelectronics technology in recent years. An integrated or hybridized silicon detection system also offers opportunities for on-board information processing. The lowest level of built-in intelligence would consist of the automatic setting of thresholds for Minimum Ionizing Particles (MIPs) and data compaction with zero-suppression. Detector systems with more intelligence, like cluster recognition or track reconstruction through two or several planes, could be called "micropattern detectors" [1].

It seems wise to attack the study and development of such devices at the front-end. Therefore, we concentrated on the question, is it possible within the power budget to make a readout circuit that is able to detect a typical charge of 10^4 electrons, (1.6 fC), which is generated by a MIP in $120\text{ }\mu\text{m}$ of silicon? The choice was made to generate only a 1-bit digital output signal. It would be possible to make also the analog signal available for readout, at the expense of extra space and power. The virtues of either approach will be briefly discussed in the conclusions. Compared to the CRC infrared DRO circuits described by Kramer et al. [2], which have passively integrating pixels, the present circuit is active and has high speed signal processing inside the pixel matrix, so that fast-or, sparse readout and other high speed logic operations are possible.

An experimental chip has been manufactured in the $3\text{ }\mu\text{m}$ p-well SACMOS process^(***) and consists of a matrix of 9×12 cells on a pitch of $200\text{ }\mu\text{m} \times 200\text{ }\mu\text{m}$. Each cell has a $65\text{ }\mu\text{m} \times 65\text{ }\mu\text{m}$ bonding pad which should allow coupling of a separate detector chip using bump bonding (fig. 1). The input is connected to a micropower amplifier, a latching comparator which operates at up to 10 MHz, and an addressable digital storage element. In the first experimental chip no further digital functions have been incorporated, and even the addressing of each element is still external. This allows flexibility in the testing of the circuit. A picture of the chip is shown in fig. 2.

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(***) The Self Aligned Contact Metal Oxide Silicon (SACMOS) process [3] is a proprietary process of Faselec AG, Zürich, a subsidiary company of Philips N.V.

Fig. 1 Schematic illustration of bump bonding between a detector chip and an electronic readout circuit. The bump metal contact may be gold, indium or solder. The metal can be deposited on one or both of the chips by evaporation or electrolytic deposition. Several additional metal layers serve as adhesives or act as barriers against diffusion of lifetime degrading metals like gold. Ionizing particles generate free charge carriers in all components of the assembly, but only in the detector chip are these carriers effectively collected.

A more detailed description of the circuit is given in the next section. The electrical characterization of the circuit is facilitated by the bottom row of cells, whose inputs are capacitively coupled to p-well contacts and eventually to a conventional bonding pad. A well-defined charge signal can thus be injected electrically. The electrical test results are presented in sect. 3. The circuit has been connected by ultrasonic wire bonding to silicon particle detectors, using the top row of cells which have enlarged bonding pads ($65\ \mu\text{m} \times 80\ \mu\text{m}$). Satisfactory results were obtained in tests with electrons and X-ray photons of energy between 22 keV and 122 keV, and the circuit is functioning as foreseen. Sect. 4 describes these particle measurements. Finally, the future work is discussed, in particular the design of a system architecture for the use of this experimental pixel cell, and the bump bonding of a matrix detector. The latter subject presents technological problems of a different kind, which might be avoided by using the electronic circuit presented here, directly on a high resistivity detector substrate.

2. CIRCUIT DESCRIPTION

The front-end circuitry associated with each pixel consists of a micropower amplifier, a latching comparator and a local

Fig. 2 Picture of the mask layout of the experimental readout circuit. The bottom row of cells can be stimulated electrically, the top row has enlarged bonding pads to enable wire bond connection to a linear test detector signal alongside the chip. All cells together can be connected using bump bonding to a matrix detector.

digital memory, as schematically presented in fig. 3. Tentative design specifications are recapitulated in Table 1. The prime concerns in the design were speed, space and power dissipation.

To reduce space and power and improve the noise, the amplified signal is shaped to reach a peak after 30 ns and is longer than 100 ns. This is allowed in particle physics applications where few pixels are hit in an event, typically ~ 100 in 10^6 , and the probability of successive hits is negligible. The result of the signal processing was designed to appear as a 1-bit digital signal after ~ 100 ns. The circuit is designed using the parameters of a well-established $3 \mu\text{m}$ p-well CMOS process. The special feature of this process is the self-aligned contacts, which enable a very dense layout [3].

Preamplifier

The schematic of the micropower amplifier is shown in fig. 4. The detector element is DC coupled to the input of a current follower which delivers the charge onto the very small stray capacitance $C_L \cong 40 \text{ fF}$. The current follower has a low input impedance, ensuring minimal crosstalk between pixels. A high charge-to-voltage gain is obtained in a single stage:

$$\Delta V \cong \frac{\Delta Q}{C_L} \approx 20 \text{ mV/fC} = 3 \mu\text{V/e}^-$$

This is possible if C_L is kept small by loading it only with a voltage follower, which in turn delivers the signal V_{out} to the comparator. The time constants T_{in} , T_L and T_{out} associated with C_{in} , C_L and C_{out} determine also the maximum signal value

$$\Delta V_{\text{max}} \cong \frac{\Delta Q}{C_L} \left[1 - \frac{T_{\text{in}} + T_{\text{out}}}{T_L} \right]$$

and the signal peaking time

$$t_{\text{max}} \cong (T_{\text{in}} + T_{\text{out}}) \ln \left[\frac{T_L}{T_{\text{in}} + T_{\text{out}}} \right] \cong 30 \text{ ns}$$

The resistance R_L (MOS transistor M2) provides for continuous resetting of the output signal level, with a decay time constant $R_L C_L \cong 100 \text{ ns}$.

Fig. 3 Block schematic of the pixel readout circuit. The current follower and the voltage follower constitute together the micropower amplifier.

TABLE 1 - Design specifications and measured characteristics

	Specification	Measured value in test
Pixel size	200 μm x 200 μm	idem
Supply voltage	3 V	3 V
Power dissipation per pixel	40 μW (100 mW cm^{-2})	30 μW
Detector pixel capacitance	$\leq 20 \text{ fF}$	up to 200 fF
Total input capacitance	$\sim 150 \text{ fF}$	up to 300 fF
Minimal detectable signal ΔQ_{min}	10^4 e^- in 10 ns	2000-5000 e^-
Noise	$< 10^3 \text{ e}^-$ r.m.s.	500 e^- r.m.s.
Shortest cycle time	100 ns	100 ns, slight problems below 130 ns
Peaking time analog signal	30 ns	30 ns
Decision time comparator	50 ns	60 ns

Fig. 4 Schematic of the analog amplifier part, showing the detector connection. V_{dd} is 3 V and V_{b0} , V_{b1} are supplied by an internal power supply, not included in this schematic. V_B is the detector bias voltage. C_{in} , C_L and C_{out} are the effective capacitances associated with the various circuit elements.

For this circuit to work properly it is essential that C_{in} , mainly consisting of the detector capacitance and the input pad capacitance, remains below ~ 300 fF. Otherwise ΔV_{max} and t_{max} are degraded and the noise increases. The equivalent noise charge (ENC) at the input is

$$ENC^2 \cong \frac{1}{2} kTC_{in}$$

$$\text{if } \frac{C_{in}}{C_L} \gg 1.$$

For 300 fF the theoretical value is $155 e^-$ r.m.s. The supply current is about $2 \mu A$ at 3 V. The simulated signals V_{in} and V_{out} are shown in fig. 5.

Fig. 5 Signals as a function of time.

Comparator

The regenerative comparator is latched by the falling edge of the master clock signal (see also fig. 5), about the time t_{max} . It then needs ~ 60 ns to produce a logic signal ($V_{ss} = 0$ V) if the threshold is exceeded. Otherwise it remains at $V_{dd} = 3$ V. The output is stored after ~ 100 ns in a static R/S flip-flop and, if positive, connects together the row and column wires corresponding to the activated pixel. The flip-flop is reset on the rising edge of the next clock pulse.

The schematic of the comparator is shown in fig. 6. The circuit operation is synchronized with the arrival of particle signals via the master clock which has a maximum frequency of ~ 10 MHz. The differential pair M6a-M6b with AC coupling via the capacitor C_{byp} (2 pF) only amplifies fast signals at the input and should be relatively insensitive to DC variations caused by bad transistor matching or a large detector leakage current. During initialisation and signal amplification in the preamplifier (~ 30 ns) this input stage is charged via the "diodes" M7a-M7b, and this is initiated by the rising edge of the clock. The falling edge activates transistors M8a-M8b, and the differential output voltage grows rapidly during the comparison.

Fig. 6 Schematic of the input stage of the latched comparator. A second flip-flop output stage serves to reach the 3 V digital output level and is not shown. The switch at the top is set as in the initialisation phase, which lasts ~ 30 ns.

The threshold is dynamically controlled by the difference of the currents I_{qa} and I_{qb} . The current $I_{qb} = 1.3 \mu A$ is derived from the general supply circuit and the pilot current I_{qa} can be set externally between $0.5 \mu A$ and $1.2 \mu A$. The reaction time of this circuit depends mainly on the time constants associated with the capacitances of nodes 4a and 4b. Simulation and reality agreed well, and ~ 60 ns is found for the nominal signal of 10^4 electrons. An output stage is added to the circuit of fig. 6, to reach a digital output level and also to return quickly to the quiescent state.

3. ELECTRICAL MEASUREMENTS

The bonding pads of the bottom row of cells are positioned above a p-well implantation, but separated from it by a 600 nm thick oxide. The dimensions are such that a 160 fF input capacitor is created and an electrical pulse of 1 mV applied to a p-well contact injects a charge of $1000 e^-$ into the preamplifier. This allows for easy electrical testing, as shown in fig. 7. While clock pulses of ~ 30 ns width are applied at 10 MHz rate, an input pulse corresponding to $10^4 e^-$ is applied, and ~ 100 ns after the input pulse the logic level at the output node is changed. For a fixed comparator threshold one can vary the input pulse amplitude, and observe the comparator output, as shown in fig. 8. The 12 curves in this plot represent the 12 cells of the bottom row of a single readout chip. The transition between 5% response and 95% response (4σ) for a single cell takes place over 2 mV. Supposing a Gaussian distribution one finds a noise of $500 e^-$ r.m.s. However, one sees immediately that the non-uniformity of the thresholds for several cells exceeds by far the noise. Before discussing the non-uniformity in some detail, we report first the threshold sensitivity for the current setting of I_{qa} in fig. 9 and the circuit response for signals that are not exactly in phase with the clock (fig. 10). The threshold variation with current setting is nearly perfectly linear and allows a precise threshold definition. The data of fig. 10 show that the threshold has nearly a plateau value for pulses within ± 5 ns of the ideal timing. Signals that are 30 ns late encounter already a very high threshold.

Threshold non-uniformity

The threshold non-uniformity observed in the electrical testing (fig. 8) limits the possibility to exploit the low noise and to detect deposited charge in the range 2000-9000 e^- in a reliable way. An investigation has been made to identify the cause of the threshold variations. By internally probing the cells it was found that the amplifier gain variations due to variations of C_L exist but are not excessive. On the contrary, the effective thresholds of the dynamic comparators vary considerably in a random way. Slight variations of geometry and oxide charge apparently lead to variations of I_{qa} and I_{qb} , which become important relative to the already small difference $I_{qb} - I_{qa}$. Several options have been identified which could reduce the threshold non-uniformity.

The problems of matching and non-uniformity had been to a certain extent anticipated, but were not of prime concern in this first experimental chip. However, it is obviously not sufficient to create a single operating unit, but one also has to make sure that all pixels in the chip operate in a controllable way, and that a large number of chips have identical characteristics. In early imaging devices like CCD similar problems arose, and correction matrices requiring extensive computational power had to be used. Recently developed CCD imaging chips in hand-held cameras do not need this any more, because of more elaborate design and above all, because of extremely homogeneous processing.

Fig. 7 Electrical testing of pixel element. The top trace is the 10 MHz master clock. The input signal in the middle injects 10^4 electrons into the preamplifier, and the comparator response at the bottom appears after ~ 100 ns, and is reset by the next clock cycle.

Fig. 8 Threshold curves of the 12 cells in the bottom row of one chip, tested by injection of an electrical pulse. The response in % is plotted as a function of input amplitude in mV. With the dimensioning of the input capacitor, 1 mV input voltage corresponds to $1000 e^-$ of input charge.

Fig. 9 The measured threshold charge as a function of the threshold $I_{qb} - I_{qa}$ for a single pixel readout cell.

Fig. 10 The measured threshold charge as a function of the time delay between the input pulse and the falling edge of the master clock pulse, which starts the comparison.

4. MEASUREMENTS WITH RADIATION

The circuit is designed for operation in synchronous mode, with particles arriving at a precisely predictable time, like it is the case in collider experiments. Testing of such a circuit with radiation is not straightforward, because particles from sources or in slow extraction beams arrive randomly in time and are only occasionally in phase with the readout clock. Active triggering is virtually impossible because of the fast operation of the circuit. The only way is a *posteriori* selection of particles which happened to be within ± 5 ns of the start of the DRO cycle, using a coincidence detector. Such a coincidence detector is just visible in the experimental setup of fig. 11a.

Two types of 300 μm thick, totally depleted detectors were used. One consists of 0.25 mm² square or circular diodes placed on a 3 x 3 mm² chip (fig. 11(a)) and the other is a silicon microstrip detector with 100 μm pitch (fig. 11(b)). Alternately one strip is connected to a pixel input, and the following one is connected to a contact plate on the circuit board (top), which can be grounded. If this contact was left floating the count rate of each pixel element increased by 60-90% as expected. The detector capacitance of the 0.25 mm² element is 90 fF and that of a microstrip 350 fF. To this has to be added ~ 100 fF for the contact pad and the wire bonding, to find the input capacitance C_{in} .

From a ¹⁰⁶Ru source 3.5 MeV electrons are impinging on the detector, and signals are easily seen, even at a high threshold setting, both in the microstrip detector and the other diodes. That the leakage current of the detector has little influence on the circuit operation could be deduced from the insensitivity to ambient light. This increases the detector current from 0.1 nA to several 100 nA.

Fig. 11 Test setup for radiation measurements. The DRO chip is mounted on a printed circuit board (PCB). The inputs are connected to silicon detector elements. (a) Square or circular elements of 0.25 mm² on a test detector chip (middle) are connected to inputs on the DRO chip (bottom). Through the hole one can just see another detector test chip, below the PCB connected to a fast integrated amplifier, which can provide an external trigger for coincident particles. (b) A silicon strip detector with 100 μm pitch connected to the DRO.

X-ray testing and noise

Testing of the circuit with X-ray photons is of interest, because it allows the determination of the threshold equivalent energy in an absolute way. Sources of ⁵⁷Co (122 keV), ²⁴¹Am (59.5 keV) and ¹⁰⁹Cd (22.2 keV and 24.9 keV) have been used, and for each source the threshold $I_{qb} - I_{qa} = \Delta I_q$

was varied in steps of $0.01 \mu\text{A}$, while the integral number of photon counts was recorded. By differentiating these integral counts, spectra were obtained as shown in fig. 12. The end points of the ^{106}Cd and ^{241}Am spectra were taken as reference points, and an absolute energy scale was determined as shown along the top axis of fig. 12, supposing that the threshold variation is linear (see also fig. 9). Each measurement bin of $0.01 \mu\text{A}$ corresponds to an energy difference of 1.4 keV . The spectra do not really show the full absorption peaks, because the signals are not synchronous with the clocking of the circuit, which ran at 5 MHz in this measurement. Out-of-phase signals are sampled before or after their peak (fig. 10) and contribute to the smearing towards low-energy. The occasional in-phase signals provide the highest energy values, and the high-energy edge of a spectrum can be used to determine a half-width, half-maximum noise figure: one or two bins. This corresponds to a FWHM of $< 4 \text{ keV}$ or $< 500 \text{ r.m.s. electrons}$. The noise in the low energy region is also indicated in fig. 12. It contributes to the spectra below 12 keV and it becomes dominant below 5 keV . These data confirm the noise values determined in the electrical testing. It should be mentioned that in this test setup the noise is not yet optimal, because the wire bonding connection to an external detector gives a higher capacitance ($200\text{--}400 \text{ fF}$) than the design value (150 fF) for a detector element connected by bump bonding.

Fig. 12 Energy spectra for ^{106}Cd and ^{241}Am photon sources, obtained by differentiation of the integral counts in a threshold scan. The energy scale on top is determined from the positions of the two end-point energies. The vertical scale gives the differential number of counts per s. The spectra are smeared towards lower energy because signals are not always sampled at the peak value.

5. CONCLUSIONS

The DRO front-end circuit operates with low power and low noise, at frequencies between 5 and 10 MHz . Using a process allowing smaller linewidth ($1 \mu\text{m}$ or $2 \mu\text{m}$) it may be possible to achieve higher frequency and smaller pixel size. The size of the pixel moreover depends on the circuitry that one wishes to include on site, and the area needed for the bump bonding. It has been reported by Hoeberechts [4] that bumps of $10 \mu\text{m} \times 10 \mu\text{m}$ on 20 to $50 \mu\text{m}$ pitch are possible nowadays, but significant cost is involved in the engineering of such technology. For the present experimental matrix it is foreseen to bump a silicon detector onto it, using either gold or indium bumps, but this is not expected to basically change the system performance, except for the lower noise. Given the measured noise value of $< 500 \text{ e}^- \text{ r.m.s.}$, a bumped silicon pixel detector could probably just detect signals as low as 5 keV or 1500 e^- .

Bumping of a separate detector chip could be avoided altogether if the detector function could be integrated in the silicon substrate wafer. Development work on CMOS processing of high resistivity wafers is undertaken at several places, but is likely to require several more years, given the funding levels which are low compared to mainstream technology development. Nevertheless, the advantages would include easier alignment and improved precision, less multiple scattering and smaller pixel size. A bumped readout circuit would have the advantage that it can also be used in connection with other types of detector material, like HgI_2 or CdTe .

It is a subject of hot debate if pixel detectors should have analog signal readout besides the 1-bit digital signal. The most commonly used argument is the need for interpolation for improved precision. We are investigating the possibility to include analog storage and readout in the present circuit, but this will increase size and power. Analog data also create an important load on peripheral electronics and on information processing, so that a careful analysis must be made before deciding to use it. On the other hand, a purely digital pixel cell could be made much smaller, and certainly interpolation in a $\sim 10 \mu\text{m}$ wide region between adjacent cells is still possible, using digital "double hits". In this way an absolute coordinate within $10 \mu\text{m}$ or $20 \mu\text{m}$ wide regions is obtained in a single plane, if $40 \mu\text{m} \times 40 \mu\text{m}$ cells could be realized.

The peripheral circuitry that has to be included in a more realistic pixel detector will depend on the use of the device. In particle physics a sparse readout is likely to be needed, as well as pipelining of addresses of hits. In imaging applications one might include scalers (counters), either inside each pixel or in an associated memory. The contents could be read out after each frame time. The pixel detector readout chips must be designed with a hierarchical detector system in mind, in order to achieve fast readout with a large detector area, up to 1 m^2 , corresponding to several 10^4 chips. Although the design of

this peripheral circuitry presents a considerable effort, it is expected to encounter less obstacles than the design of the front-end circuit in the pixel itself, where difficult trade-offs had to be made.

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