Test of Radiation-Hardness of CMOS Test Structures in Neutron and Proton Beams

Santa Cruz Institute for Particle Physics
University of California Santa Cruz
Santa Cruz, CA 95064

C.M. Hoffman, D. Holtkamp, W.W. Kinnison, C. Millner, W.F. Sommer, H.J. Zlock
Los Alamos National Laboratory
Los Alamos, NM 87545

P. Ferguson
University of Missouri-Rolla
Rolla, MO

P. Giubellino, S. Sartori
INFN Torino
Turin, Italy

One of the main requirements for SSC/LHC front-end electronics is to be radiation-resistant. The SSC Workshop on Radiation Levels in the SSC[1] found that, for example, a silicon tracking device at a radius of 8 cm has to survive about 1 MRad and a few 10^{12} neutrons/cm^{2} per year at the design luminosity of 10^{33} cm^{-2}sec^{-1}.

For our program to develop a large tracking device based on Si p strip detectors for the SSC,[2] an important part is the identification of radiation hard VLSI technologies for the front-end electronics. The analog amplifier-comparator is being fabricated in dielectric isolated (D.I.) bipolar technology[3] for low noise and speed and radiation-hardness.[3] The pipe lining of the data requires a low power technology and thus form we are building a digital time slice chip (DTSC) in the form of a SRAM in CMOS.[4] There is a question as to the radiation-hardness of MOS transistors under irradiation by ionizing particles[5] and neutrons.[5] On the other hand, radiation-hard CMOS processes have been developed in the last years and are now commercially available.[5]

To compare different CMOS technologies, we have tested the radiation resistance of various VLSI technologies at Los Alamos National Laboratory. We have reported[9] before on the irradiation of n and p transistors on 2 \mu m CMOS test structures with neutrons in the LAMPF neutron spallation source and we will remember only a few results. For digital application the radiation damage to CMOS transistors is characterized by a shift of the threshold voltage, i.e., the gate voltage at which the transistor turns on. Figure 1 shows the dependence of the threshold voltage on the neutron fluence for two different technologies. Figure 1a is a non-hard p transistor from ORBIT[9] and fig. 1b is a hard p transistor from UTM.[11] The superior radiation resistance of the hard-rad transistor (fig. 1b) is obvious. We concluded that rad-hard devices from UTM survive even fluences of 10^{15} n/cm^{2}.

We now have extended out measurements to exposures in the 800 MeV LAMPF proton beam.[12] We have tested transistors of 1.2 \mu m feature size produced by UTM. The data in figs. 2 and 3 represent the threshold voltage shifts \delta V_{th} after doses of 3 MRad (10^{14} protons/cm^{2}) as a function of transistor sizes and for a different biasing condition during irradiation. The observed threshold voltage shifts for worst case biasing are of the order of \delta V_{th} \approx 150m\text{V} for p transistors (fig. 2b) and \delta V_{th} \approx 250m\text{V} for n transistors (fig. 3b). They show that the UTM process is radiation hard into the many MRad. In its performance let us expect that it will offer sufficient radiation resistance for application in the SSC, LHC and IHERA.

REFERENCES

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**Fig. 1.** a) Threshold voltage $V_{th}$ vs. neutron fluence for the non-radi-hard $p$ transistor #2 manufactured by ORBIT. b) Threshold voltage $V_{th}$ vs. neutron fluence for the radi-hard $p$ transistor #7 manufactured by UTMC.
Fig. 2. Threshold voltage shift $\Delta V_{th}$ for UTMC $p$ transistors of various sizes (width/length) after a dose of $10^{14}$ protons/cm$^2$ for different biasing conditions: a) floating, b) $V_{Gate} = V_{Substrate} = -5\ V$, c) $V_{Gate} = V_{Substrate} = 5\ V$.

Fig. 3. Threshold voltage shift $\Delta V_{th}$ for UTMC $n$ transistors of various sizes (width/length) after a dose of $10^{14}$ protons/cm$^2$ for different biasing conditions: a) floating, b) $V_{Gate} = V_{Substrate} = 5\ V$. 