The TileCal Upgrade Readout Architecture

- Prototype Development Program for the Phase 2 Upgrade
- Replacement of All Front-End & Back-End Electronics
- 3 Front-End Technologies being Considered for PMT Readout:
  - 3-in-1 (Discrete Design)
  - FATALIC (Custom ASIC)
  - QIE: Charge Integrator and Encoder Custom ASIC, 350 nm SiGe

Overview of the QIE12

- "Current Splitter" with Gated Integrator
  - No Pulse Shaping
  - Pseudo-Logarithmic Response
- Pipelined Operation; Dead-timeless at 40 MHz
- 18-bits Dynamic Range
- 1.5 - 3 pC Least Count
- Internal TDC → 1 ns resolution
- Internal Shunt for External Current Integrator
- Internal Charge Injection
- Low Power – 360 mW/ch (Chip Only)
- Highly Integrated; Simple Interface & Support Circuitry → High Reliability
- Radiation Tolerant (SiGe Process for TID; SEU-Tolerant Design)
- 50 Ohm Input, Incorporate SPI for Slow Control
- Allows for one data bus for all slow control functions: Integrator ADC; Q Inj DAC, QIE

Current Integrator Implementation

- Design in Progress
- Test Beam Starting
- Technology Decision: Summer, 2016

A Few Measurements & Results on Prototype Chips

- Current SEE Performance
  - ~1 SEU Error per 3E+8 p/cm² per chip
  - ~1 Fake Hit per 1E+9 p/cm² per chip
  - No Errors in Shadow Register (SEU-Hard)
  - Est 10 yr Dose: ~4E+9 p/cm²

- DC Current Monitor
  - 38 pA/Count
  - Current Monitor Pedestal
  - Range 1 Shown Sense for all Ranges

- Programming Interface
  - SPI Serial Peripheral Interface
  - (M4) Serial Register

- Reconstructed Charge
  - Response of the QIE chip. All Gain f/As are combined.