Metrological Characterization of an Ultra-low Noise Acquisition System for Fast Voltage Pulses Measurements

Pasquale Arpaia1,2, Carlo Baccigalupi1,3, Michele Martino1,
1TE Department, CERN Geneve, 23 Switzerland
2EN Department, University of Sannio, 82100 Benevento, Italy
3PH Department, University of Calabria, 87036 Rende (CS), Italy

Keywords:

Abstract

The metrological characterization of a custom designed ultra-low noise analogue front-end for an acquisition system for the measurement of flat-top of fast voltage pulses is presented. The system has challenging requirements, in particular for Common Mode Rejection Ratio (CMRR), thus custom methods have been defined, by illustrating the experimental results achieved at the European Organization for Nuclear Research (CERN) during the study of the new Compact Linear Collider (CLIC).

Presented at: I2MTC, 2015

Geneva, Switzerland
October 2015
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Pasquale Arpaia
TE Department
CERN, Geneve, 23 Switzerland
Electrical Engineering and Information Technologies Department
University Federico II
Naples, Italy
Email: pasquale.arpaia@cern.ch

Carlo Baccigalupi
TE Department
CERN, Geneve, 23 Switzerland
Electrical Engineering and Information Technologies Department
University of Calabria
87036 Rende (CS), Italy
Email: carlo.baccigalupi@cern.ch

Michele Martino
TE Department
CERN, Geneve, 23 Switzerland
Email: michele.martino@cern.ch

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I. INTRODUCTION

Pulsed power supplies are widely used when power consumption has an important impact on the feasibility of the application [1]; this is the case, among others, of pulsed lasers, electromagnetic pulse generators, or even particle accelerators [2]. In this framework, the full characterization of the power pulses is needed in order to, for instance, predict the exact amount of energy delivered to the load. The state of the art for pulse measurements is mostly dedicated to ultra-fast pulses in the nanosecond regime (or even sub-nanosecond) as highlighted by the National Institute of Standards and Technology (NIST) [3]; in addition, the reference standard [4] is mostly (or entirely) dedicated at the evaluation of the pulse parameters, which are critical for many industrial fields as discussed in [5] and [6] where both procedures and definitions are given. However, new and more demanding applications arise from particle accelerators for high-energy physics. At CERN, a new linear accelerator is currently under study, the Compact LInear Collider (CLIC); its klystrons will be supplied by high-voltage modulators in pulsed mode. The required experimental precision is achieved by a careful characterization of the high-voltage pulses [7]. For this reason, an ultra-low noise acquisition system has been designed and developed at CERN [8]. In this paper, the preliminary metrological characterization of the above mentioned acquisition system, with special focus on the common mode rejection evaluation, is presented. In particular, the test setups and the obtained results are illustrated.

II. THE ACQUISITION SYSTEM

Directly derived from the accelerator performance, it is required a flat-top pulse-to-pulse repeatability better than 100 ppm to be verified over a total bandwidth of 5 MHz [7]. In order to measure this parameter a measurement chain composed by a high voltage divider, to convert the high-voltage pulses into 10 V ones, and an ultra-low noise acquisition system have to be designed. The acquisition system is composed by an analog front-end, reported in Fig.1, and the state-of-the-art acquisition board NIPX1 – 5922.

By specification, the interest is completely focused on the pulse flat-top, thus the basic working principle of the front-end is to subtract the nominal DC value of the flat-top from the pulse. In this way, the flat top is translated around zero and the Full Scale of the acquisition board is almost entirely dedicated to the flat-top measurement [8], taking full advantage of its high resolution. In order to accurately center the flat-top around zero, the differential stage of Fig.1 (highlighted by the red dotted circle) has to show an adequate Common Mode Rejection Ratio (CMRR); in fact a residual DC common mode voltage, left to the downstream amplification (50 V/V), could bring the flat-top far from zero (or even out of scale).

III. COMMON MODE REJECTION RATIO

The CMRR expresses the ability of a differential circuit of rejecting common mode input voltages. In the following, the experimental assessment of the CMRR (A) between the inputs, and (B) between the references is reported.

A. Between the inputs

In its nominal working conditions, the acquisition system will have a 10 VDC on the IN– input and a 10 V pulse waveform on the IN+ input (Fig.1). Therefore the differential stage has to be designed for properly rejecting a DC common mode
input up to 10 V. This test allows evaluating the DC CMRR of the analog front-end. When using a difference amplifier, a critical parameter for its Common Mode Rejection Ratio, CMRR$_{\text{diff}}$, is the uncertainty of the feedback resistors ratio \cite{10}; that’s why, in \cite{8}, a CMRR$_{\text{diff}}$ higher than 86 dB was declared to be achievable with a 0.01\% relative uncertainty resistors network (RN2 in Fig.1) for the differential stage. This statement is proved experimentally by means of the test setup of Fig.2. The multifunction calibrator Wavetek 4808 generates a DC voltage ranging from 2 V to 10 V (in steps of 2 V) which is applied to both the inputs of the analog front-end under test. Thus, at each step, a common mode voltage equal to the voltage generated by the Wavetek 4808 is seen by the circuit. At this stage, the interest is entirely dedicated to the DC CMRR$_{\text{diff}}$, therefore, an RC low-pass filter is used to cut-off disturbances above 20 Hz ($R = 820 \, k\Omega$, $C = 10 \, nF$).

The first test step consists in measuring the offset corresponding to a common mode input voltage of 0 V. This is achieved by disconnecting the multifunction calibrator from the setup of Fig.2 and then measuring the output offset with shorted and grounded inputs. The next steps consist of measuring the output offset corresponding to a particular input common mode voltage ($V_{O2}, ..., V_{O10}$). In Table I, the averaged results of 30 repeated measurements with their standard deviations are reported. At this point, the CMRR$_{\text{diff}}$ is assessed as:

$$\text{CMRR}_{\text{diff}} = 20 \log_{10}\left(\frac{G \cdot V_x}{|V_{O2} - V_{O10}|}\right)$$ (1)
where $G$ is the differential gain of the front-end ($G = 50 \, V/V$), $V_x$ is the common mode input, $V_{Ox}$ the output offset measured with $V_x = 0 \, [V]$ at the inputs, and $V_{Osc}$ the output offset measured with both the inputs shorted to ground (first step). The $CMRR$ derived by equation (1) is thus reported in Fig.3 with its standard deviation. The worst case is observed at the nominal working condition of the measurement system with a common mode input of $10 \, V$. In this case, a $DC \, CMRR_{diff}$ of about $87.7 \, dB$ is measured, which confirms the theoretical prediction in [8]. Indeed, the test setup measures the $CMRR_{diff}$ of the whole circuit not only the one of the difference amplifier. Thus, if the worst-case condition is met by the whole $CMRR$, a fortiori it will be met by the difference amplifier.

B. Between the references

In high-precision applications, all the measurements have to be referred to the same reference voltage (e.g. $GND$). However, when two or more sources are far, this cannot always be guaranteed. In this case, ground loops could occur and, as a consequence, unwanted currents circulate into the measurement chain accordingly affecting its metrological performance. The input stage of the analog front-end under test is composed by a differential sensing circuit (blue dotted circle in Fig.1) [8], rejecting the common mode voltage between the two grounds. The test setup of Fig.4 allows this $CMRR_{ref}$ to be assessed versus the frequency. In particular, in the previous section, $CMRR_{diff}$ was assessed by imposing a common mode voltage between each input and $GND$, while now the common mode voltage is imposed between the references of the two $DC$ generators. A Transfer Function Analyzer (TFA) Powertek GP 102 generates a set of sine waves of small amplitude ($20 \, mV_{pp}$) with frequency ranging from $10 \, mHz$ and $1 \, MHz$. The sine waves are imposed as common mode between the references of two $10 \, V$ reference portable generators ($PBCs$) [11], whose output signals are given as inputs to the front-end (in this test the static working point is fixed at $10 \, V$). The input amplitudes of the sine waves and the front-end output are then measured by the TFA.

The resulting Bode diagram (Fig.5) shows a $CMRR_{ref}$ well above $90 \, dB$ up to about $1 \, kHz$. As expected, at higher frequency, the $CMRR_{ref}$ rapidly decreases to about $55 \, dB$ at $1 \, MHz$, which is still a considerable result.

IV. AMPLITUDE FREQUENCY RESPONSE

By specification, the pulse-to-pulse repeatability has to be verified over a total bandwidth of $5 \, MHz$, thus the aim of this test is to verify that the analog front-end has a bandwidth of at least $5 \, MHz$. The TFA used for $CMRR$ measurements has a range of $2 \, MHz$, thus, the new setup in Fig.6 is needed. It consists of an arbitrary waveform generator (Agilent 33220A) and two digital multimeters (HP 3458A) set in AC voltage mode. The multimeters were firstly characterized up to $10 \, MHz$ (their maximum frequency in AC voltage mode), by measuring a worst-case amplitude difference smaller than $0.6 \, dB$. A set of small-amplitude sine waves ($20 \, mV_{pp}$) with frequency ranging from $10 \, kHz$ to $10 \, MHz$ is generated by the arbitrary waveform generator and applied to both the multimeter and the analog front-end. The second multimeter is connected to the front-end output. At each step, the $RMS$ values of the analog front-end input and output signals are measured by the two multimeters. After the first set of measurements, the two multimeters are swapped and the results obtained in the two configurations averaged in order to compensate possible systematic errors. The resulting Bode diagram of Fig.7 highlights a good flatness up to $5 \, MHz$, where the $-3 \, dB$ point is located.

In conclusion, the result of this test confirms a satisfying flatness of the amplitude response of the circuit with a bandwidth of about $5 \, MHz$. Nevertheless, the $DC$ gain of the front-end was assessed to be $49.95 \, V/V$ in satisfying agreement with design specification of $50.00 \, V/V$.

V. STEP RESPONSE

The delay introduced by the analog front-end with an input small step of $20 \, mV$ is measured through the setup in
The input step is generated by the arbitrary waveform generator Agilent 33220A with a rise time of 100 ns. The step is applied both to channel 0 of the oscilloscope (Tektronix MSO 4101) and to the analog front-end, while the front-end output is measured on the channel 1.

In Fig. 9, the test result is depicted; by considering the time between the 50% of the transitions, a delay smaller than 150 ns can be observed.

VI. CONCLUSIONS

The metrological characterization of an ultra-low noise analogue front-end for fast voltage pulses flat-top measurement has been presented. Given the working principle of the system, the CMRR turned out to be one of the most critical performance to be verified. The theoretical prediction of CMRR in [8] was confirmed by the experimental results.

The future step of this research work is to evaluate the temperature coefficient of the acquisition system in order to verify that temperature does not jeopardize the system performance.

ACKNOWLEDGMENT

The Authors would like to thank Miguel Cerqueira Bastos for his collaboration and precious advices.

REFERENCES


