Enhanced analogue front-end for the measurement of the high state of wide-band voltage pulses with 87 dB common-mode rejection ratio and ± 0.65 ppm 1-day offset stability

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Keywords:

Abstract

An improved analogue front-end for measuring the high state of trapezoidal voltage pulses with transition duration of 3 μ s is presented. A new measurement system, composed by a front-end and the state-of-the-art acquisition board NI PXI-5922, has been realized with improved Common Mode Rejection Ratio (CMRR) of more than 87 dB at DC and 3-sigma stability of ± 0.65 ppm over 1 day. After highlighting the main design enhancements with respect to state-of-the-art solutions, the CMRR measurement is reported. The output drift due to temperature and humidity is assessed to be negligible. Finally, the worst-case repeatability is measured both with shorted-to-ground inputs and with an applied common-mode voltage of 10 V, which represents the nominal working condition. C 2015 AIP Publishing LLC. [<http://dx.doi.org/10.1063/1.4930553>]

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Enhanced analogue front-end for the measurement of the high state of wide-band voltage pulses with 87 dB common-mode rejection ratio and ± 0.65 ppm 1-day offset stability

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An improved analogue front-end for measuring the high state of trapezoidal voltage pulses with transition duration of $3\ \mu\text{s}$ is presented. A new measurement system, composed by a front-end and the state-of-the-art acquisition board NI PXI-5922, has been realized with improved Common Mode Rejection Ratio (*CMRR*) of more than 87 dB at *DC* and 3-sigma stability of ± 0.65 ppm over 1 day. After highlighting the main design enhancements with respect to state-of-the-art solutions, the *CMRR* measurement is reported. The output drift due to temperature and humidity is assessed to be negligible. Finally, the worst-case repeatability is measured both with shorted-to-ground inputs and with an applied common-mode voltage of 10 V, which represents the nominal working condition. © 2015 AIP Publishing LLC. [<http://dx.doi.org/10.1063/1.4930553>]

I. INTRODUCTION

Pulsed power supplies are widely used in applications where energy consumption is important,¹ such as pulsed lasers, electromagnetic pulse generators, and particle accelerators.² In this framework, a full characterization of the power pulses is needed, for instance, to determine the exact amount of energy delivered to the load.

Past research on pulse measurements is mostly dedicated to ultra-fast pulses in the nanosecond regime (or even sub-nanosecond), as highlighted by the National Institute of Standards and Technology (*NIST*).³ In addition, the IEEE standard 181-2011⁴ is mostly (or entirely) devoted to the assessment of the pulse parameters. In fact, they turn out to be critical for many industrial fields,⁵ as discussed in Refs. 6 and 7 where both definitions and procedures are given. However, new and more demanding applications arise from particle accelerators for high-energy physics. At *CERN*, a new linear accelerator is currently under study, the Compact Linear Collider (*CLIC*). Its klystrons will be supplied by high-voltage modulators in pulsed mode.⁸ RF power quality directly affects the machine performance; therefore, a pulse-to-pulse repeatability better than ± 100 ppm out of the high-voltage modulator is required.⁹ This needs to be guaranteed in the range of frequencies 6 kHz up to 5 MHz. For this reason, an ultra-low noise acquisition system was designed and developed at *CERN*.¹⁰ It is composed by a high-voltage divider converting the initial high-voltage down to 10 V, a custom analogue front-end and the acquisition board NI-PXI 5922. This work focuses on the low-voltage section only; thus, the high-voltage divider is not discussed. However, the voltage divider must comply with the short term stability, equivalent resistance (for thermal noise), and bandwidth requirements of the *CERN* application. Despite the fact that the low-voltage section of the instrument¹⁰ met

these requirements, some of its performance capabilities are no longer adequate because of newer very-stringent requirements adopted by *CERN*. Moreover, after the proof-of principle demonstration reported in Ref. 10, a more comprehensive metrological characterization for assessing the most critical specifications of Common Mode Rejection Ratio (*CMRR*)¹¹ and temperature dependencies¹² needed to be performed.¹³

In this paper, an analogue front-end with improved *CMRR* and thermal stability for characterizing the high states (nominally constant valued levels) of trapezoidal voltage pulses with transition durations of $3\ \mu\text{s}$ is presented. In Section IV, after detailing the improvements of the instrument, its complete metrological characterization is discussed. In particular, in Section IV, the *CMRR* measurement is reported, by presenting the experimental setup and the results. In Section V, the offset drift is assessed in a climatic chamber by means of four different measurements, highlighting dependency on both temperature and humidity. In Section VI, the Worst-Case Repeatability (*WCR*)¹⁴ is measured both with shorted-to-ground inputs (Subsection VI A) and with an applied common mode voltage of 10 V (Subsection VI B), which is its nominal working conditions.¹⁰

II. REQUIREMENTS

The acquisition system is composed of an improved analogue front-end (Fig. 1) and the state-of-the-art acquisition board NI PXI – 5922.¹⁵ For this measurement, the purpose of the front-end is to subtract the nominal *DC* value of the pulse's high state from the pulse (zero translation) and then amplify the result to adapt the full-scale of the acquisition board to the high state measurement.¹⁰ The main feature of the measurement system presented in Ref. 10 was a very-low Power Spectral Density (*PSD*) of roughly $14\ \text{nV}/\sqrt{\text{Hz}}$ resulting in an ultra-low noise measurement capability of 3.12 ppm *RMS* of full-scale even at the required high-bandwidth of 5 MHz.

However, more stringent performance requirements arose from deeper investigations on the actual working conditions of

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FIG. 1. The analogue front-end.

the system and from *CLIC* requirements evolution. In particular, if an adequate *CMRR* value is not achieved, the differential stage (red dotted circle in Fig. 1) would not perform an effective subtraction. Furthermore, given the harsh work environment, the dependency of system performance on environmental changes and conditions must also be investigated.

III. DESIGN ENHANCEMENTS

The new performance requirements were satisfied mainly by using the two circuits highlighted by dotted circles in Fig. 1. The first circuit, highlighted in red, exploits an array (*RN2*) of matched resistors with 0.01% of relative tolerance with the following advantages:

- considerably enhance *CMRR*¹⁶ by reducing the possible unbalance of the two branches of the differential stage (red dotted circle in Fig. 1);
- stabilize gain by integrating all the temperature-sensitive gain-setting resistors into the same chip.

The second circuit, highlighted in blue, uses a differential sensing circuit on the input stage, with the following twofold advantages:

- rejection of the common-mode voltage between the analogue front-end and the upstream voltage divider,¹⁰ which could arise from the ground loop between the two different grounds, by means of another high-precision resistors network *RN1* with 0.01% of relative tolerances;
- complete decoupling of the voltage divider from the analogue front-end by means of two input buffers.

IV. CMRR MEASUREMENT

During the design of the front-end, particular attention was paid to the design of a high-*CMRR* differential stage.¹⁰

In particular, the *DC CMRR* turned out to be an important feature to properly shift the high state of the pulse to around zero. In the following, the *CMRR* measurements aimed at experimentally proving the achievement of the above-mentioned design goal are reported.

A. Common-mode input voltage rejection

A *CMRR* higher than 86 dB was expected in Ref. 10 because of the 0.01% tolerance resistors. Such a design expectation was proven by means of the setups in Fig. 2. The high-resolution (up to 24 bits) high-speed (up to 15 MS/s) acquisition board NI PXI 5922 acquires 30 records of the front-end's offset with a trigger at 50 Hz (20 ms period). Each record is composed by 2250 samples (150 μ s at 15 MS/s, namely the nominal working conditions). The test was carried out in two phases:

- The first phase (Fig. 2(a)) consisted of measuring the output offset of the front-end when both inputs are shorted to ground. An offset of about $V_{Osc} \approx -16$ mV is shown for an input common mode voltage of $V_0 = 0$ V (shorted and grounded inputs).
- The second phase (setup in Fig. 2(b)) consisted of measuring the output offset ($V_{Ox} = V_{O2} \dots V_{O10}$) corresponding to a particular input common mode voltage. A variable DC voltage source was used to generate a DC voltage $V_x = 2.0 \dots 10.0$ V (2.0 V steps) that was simultaneously applied to both inputs of the analogue front-end. At this stage of the measurement, the focus of interest was on the *DC CMRR* of the differential stage (red dotted circle in Fig. 1), namely, *CMRR_{diff}*. Therefore, a *RC* low-pass filter ($R = 820$ k Ω , $C = 10$ nF) was used to remove disturbances with frequency content above 20 Hz. At each step, a common-mode voltage equal to the voltage generated by the calibrator was applied to the circuit.

FIG. 2. Setup for measuring $CMRR_{diff}$, with inputs: (a) shorted to ground, and (b) supplied by DC voltage.¹³

In Fig. 3, the results of the repeated measurements are depicted with the errors bars representing the standard deviation (30 measurements for each point) due to wide-band noise.

The Common-Mode Input Voltage Rejection $CMRR_{diff}$ can be computed using

$$CMRR_{diff} = 20 \log_{10} \left(\frac{G \cdot V_x}{|V_{Ox} - V_{Osc}|} \right), \quad (1)$$

where G is the gain of the front-end ($G = 50$ V/V), V_x is the corresponding common-mode input, and V_{Ox} and V_{Osc} are the offsets measured when x V are applied to the inputs, and when both the inputs are shorted to ground (first phase), respectively.

In Fig. 4, the $CMRR$ is reported by highlighting the $1-\sigma$ dispersion over 30 samples. The worst case was observed with a common mode input of 10 V, which is the nominal working condition of the measurement system. As explained in Ref. 17, the offset voltage of an operational amplifier is affected by the bias point of its input differential pair, which in turn is affected by the imposed common-mode input voltage. This results in a $CMRR$ variation with respect to the particular working point. At 10 V, a DC $CMRR_{diff}$ of about 87.7 dB was measured,

confirming the theoretical prediction in Ref. 10. Nevertheless, the test setup measured the $CMRR_{diff}$ of the circuit as a whole (not only the difference amplifier as in Ref. 10); thus, if the worst-case condition is met by the whole $CMRR$, *a fortiori* it will be met by the difference amplifier.

B. Common mode ground voltage rejection

In metrological applications, all the measurements have to be referred to the same reference voltage (e.g., GND voltage); otherwise, ground loops could affect the measurement quality (Fig. 5).

The input stage of the analogue front-end is composed of a differential sensing circuit (in blue in Fig. 1),¹⁰ which rejects the common-mode voltage between the two grounds. This common mode voltage is $CMRR_{ref}$. The test setup of Fig. 6(a) allows $CMRR_{ref}$ to be assessed over a frequency range of 1 MHz. Case in comparison with the previous measurement, where $CMRR_{diff}$ was evaluated by imposing a common-mode voltage between each input and GND , in this test the common mode voltage was imposed between the references of the two DC generators. A Transfer Function Analyzer, TFA

FIG. 3. Measured output offset (V_{Ox}) vs common-mode input voltage (V_x). Error bars show the standard deviation for the 68% confidence interval ($1-\sigma$).

FIG. 4. $CMRR$ vs common-mode input voltage ($1-\sigma$ uncertainty band).¹³

FIG. 5. Ground loop between two far grounds.¹³

(also known as frequency response analyzer or gain phase analyzer), Powertek GP 102 was used to generate a set of sine waves ranging in frequency from 10 mHz to 1 MHz. The sine waves were applied between the chassis references of two fully floating DC 10 V portable generators (PBCs).¹⁸ The two PBCs, in turn, fed the two inputs of the front-end fixing the static working point at 10 V. Amplitude and phase (difference) of the input sine waves (connected to CH1 by means of a tee connection) and the output of the front-end were then measured by the TFA in order to determine the Bode diagram.

In this test, PBC 1 was used to emulate the signal coming from the voltage divider and PBC 2 the local 10 V reference voltage. In the test setup of Fig. 6(a), it is shown that the chassis of PBC 1 is connected to the terminal minus of V_{signal} on the front-end, which is a differential input. On the contrary,

FIG. 6. (a) $CMRR_{ref}$ measurement setup and (b) CM_{ref} definition.

the chassis of PBC 2 is connected to the front-end's ground through the shield of the twisted shielded pair. Fig. 6(b) shows how V_{AC} was combined at the input stage and highlights the common mode voltage (V_{CM}) which was actually experienced by the front-end,

$$V_{CM} = \frac{V_{IN+} + V_{IN-}}{2} = \frac{(V_{PBC1} + V_{AC}) + V_{PBC2}}{2} = 10 \text{ V} + \frac{V_{AC}}{2}. \quad (2)$$

The DC part of Equation (2) (10 V) was rejected according to Section IV A while the rejection of $V_{AC}/2$ was the actual purpose of this test. In a way similar to the $CMRR_{diff}$ in (1), $CMRR_{ref}$ can be defined as

$$\begin{aligned} CMRR_{ref} &= 20 \cdot \log_{10} \left(\frac{G_D}{G_{CM}} \right) = 20 \cdot \log_{10} \left(\frac{G_D V_{CM}}{V_{out}} \right) \\ &= 20 \cdot \log_{10} \left(\frac{G_D V_{AC}}{2 \cdot V_{out}} \right) \\ &= 20 \cdot \log_{10} \left(\frac{G_D V_{AC}}{V_{out}} \right) - 20 \cdot \log_{10}(2), \end{aligned} \quad (3)$$

where G_D and G_{CM} are the differential and common-mode gains, respectively. This shows that a correction factor of $-20 \cdot \log_{10}(2)$ should be applied to the instrument reading.

Given the importance of $CMRR$ for this particular work, the measurement reproducibility was tested using different test instruments and test conditions:

- two different input sine waves amplitude were applied (1 V_p and 100 mV_p);
- two TFAs were used (same model, different serial numbers);
- a Vector Network Analyser (VNA), was used thanks to its gain-phase features (model Keysight E5061B).

The results obtained were always within $\pm 0.4\%$ of each other's nominal values. In the last case, due to the VNA frequency limitation, the lowest analyzed frequency was 5 Hz.

The results obtained over 10 repetitions with both the TFA and VNA are depicted in Fig. 7, where the average value

FIG. 7. $CMRR$ of the circuit for rejecting common mode voltage between the voltage divider and the local ground.¹³

FIG. 8. Test setup for offset drift measurement.

together with the minimum and maximum bars are shown. They show a $CMRR_{ref}$ of about 87 dB up to 1 kHz, decreasing at higher frequencies down to 48 dB at 1 MHz, which is still a considerable result.

V. OFFSET DRIFT

The output drift of the analogue front-end, with an applied common mode voltage of 10 V, was characterized by means of the test setup in Fig. 8. The analogue front-end was placed inside a climate-controlled chamber, and the output voltage, corresponding to a 10 V_{DC} common mode input (PBC), was measured by a digital multimeter *HP 3458A* thanks to its DC accuracy of 0.6 ppm. The multimeter was set with a measurement time of 1 s, corresponding to a Number of Power-Line-Cycles ($NPLC$) of 50. In this way, the effect the high-frequency noise is mitigated by averaging the measurand over 1 s, and only the slow trend of the offset is assessed. In this section, the output voltage when both analogue front-end inputs are set to 10 V is referred to as offset. The following test results for (i) *offset in nominal conditions*, (ii) *temperature slow variation*, (iii) *temperature fast variation*, and (iv) *humidity response* are illustrated.

A. Offset in nominal conditions

The first test aimed at assessing the offset of the instrument during its nominal working conditions when normal operations (as power-up) or unwanted power-supply drops occur at a fixed and controlled temperature of 23 °C and relative humidity

of 30%. The test was carried out in four phases, corresponding to four different sources of offset variations: (1) *not powered*, (2) *powered*, (3) *constant power supply*, and (4) *power supply drop*. In Fig. 9, the result of the test as a whole is reported by highlighting the four steps.

- *Step 1.* The test started with the analogue front-end not powered which is resulted in an offset voltage of about -470 ppm of the full-scale (all the reported values are referred to the input). See Fig. 10.
- *Step 2.* When the power supply was turned on, the offset rapidly increased from the initial value up to about -24 ppm with floating inputs. See Fig. 10.
- *Step 3.* When the PBC was connected to both the inputs the offset moved to its nominal value of about -65 ppm (see Fig. 11) showing a very good peak-to-peak low-frequency stability of about 1.3 ppm for more than 20 h.
- *Step 4.* A voltage drop was emulated in the power supply; in particular, the nominal ± 15 V were symmetrically decreased to ± 14 V. In this case, the offset level suffered a drop of about 6 ppm for a supply variation of 1 V highlighting a good Power Supply Rejection Ratio ($PSRR$) of about 84 dB. Finally, the supply voltage was increased again to ± 15 V and the offset returned to its nominal value of about -65 ppm. See Fig. 12.

B. Slow temperature variation

The slow temperature variation test consisted in imposing a temperature profile with slow variations (30 °C in 6 h), at a

FIG. 9. Overall measurement.

FIG. 10. Power-up.

FIG. 11. Stability.

constant relative humidity of 30%, while measuring the offset by a digital multimeter *HP 3458A* (Fig. 8). In this case, an output variation of about 1.5 ppm was measured over the total temperature variation of 32 °C (Fig. 13). Correspondingly, even if there was not an instantaneous correlation between temperature and offset voltage (e.g., there is a delay), a temperature coefficient better than about 0.05 ppm/°C with a temperature variation rate of 5 °C/h could be derived.

C. Fast temperature variation

The dependence of the offset on the temperature rate is demonstrated by the fast temperature variation test. Starting from 23 °C, the temperature was increased at a rate of 10 °C/h (double the rate of the previous test) up to about 43 °C at a constant relative humidity of 30%. In this case, an offset variation of about 2.0 ppm was measured (see Fig. 14), higher than 1.5 ppm obtained in the previous test over 30 °C of variation. In conclusion, a temperature coefficient better than 0.1 ppm/°C was derived from the measurement with a temperature variation rate of 10 °C/h.

D. Humidity response

The analysis of the offset dependence on the environmental conditions was completed by assessing the relative

FIG. 12. Power supply drop.

FIG. 13. Offset variations (right-hand scale in green) due to a 5 °C/h temperature profile (left-hand scale in blue).

humidity (*RH*) response of the instrument. In particular, the test consisted of producing a humidity step from 30% to 70% while keeping temperature stable at 23 °C. A maximum drift of only 0.4 ppm was observed (Fig. 15), even over such an important humidity change. The acquired offset values shown in Fig. 15 were digitally filtered highlight the low-frequency trend due to humidity variations. In conclusion, the sensitivity of the analog front-end to humidity is less than 0.4 ppm/% RH, which is considered negligible for the CERN application.

VI. WORST-CASE REPEATABILITY

The test setup of Fig. 2, already used for $CMRR_{diff}$ measurement in Sec. IV, was used for assessing the *WCR* defined as

$$WCR(j) = \max_i |V_{i,j} - V_{i,j+1}|, \quad (4)$$

where $V_{i,j}$ is the i th sample of the j th pulse, whereas $V_{i,j+1}$ is the homologous sample belonging to the following pulse.¹⁹ The measurement was carried out by acquiring 15 000 records of the analogue front-end output, each of them composed by 2250 samples. For each of the 15 000 acquisitions, the maximum observed value was recorded. All these values were

FIG. 14. Offset variations (right-hand scale in green) due to a 10 °C/h temperature profile (left-hand scale in blue).

FIG. 15. Offset variations due to a humidity change from 30% to 70%.

used to build a histogram of the WCR in order to highlight its sample mode.

In the following, the test results for: (i) *short circuit*, (ii) $10 V_{DC}$ *common mode*, and (iii) *distribution mode vs common-mode input* are illustrated.

A. Short circuit

The test setup of Fig. 2(a) was used for this first test. The two inputs were shorted together to ground in order to measure only the contribution of the analogue front-end and the acquisition board to the WCR figure. Fig. 16 shows the histogram of the worst-case values of 15 000 acquisitions, which has a mode of about 18.7 ppm of full-scale and a highest value worst-case value well below 30 ppm.

B. $10 V_{DC}$ common mode

This test, whose setup is depicted in Fig. 2(b), allowed the WCR of the measurement system to be assessed in its nominal working conditions, with a common-mode voltage of 10 V imposed at the input. The input voltage was generated by the PBC. An RC low-pass filter, connected to the output of the PBC, attenuated the noise frequency content more than

FIG. 16. Worst-case repeatability histogram with both input shorted to GND.

FIG. 17. Worst-case repeatability histogram with both input connected to a PBC.

about 20 Hz; thus, only the DC was assumed as input of the front-end. The histogram for this WCR measurement is shown in Fig. 17 and was compatible to the one obtained with shorted and grounded inputs. This was also confirmed by a χ^2 Kolmogorov-Smirnov test at the significance level $\alpha = 5\%$ and aimed at verifying that the two independent statistical samples have the same underlying distribution, thus confirming the expected CMRR performance of the circuit.

C. Distribution mode vs common mode input voltage

The WCR test was also carried out for inputs ranging from 0 V_{DC} to 10 V_{DC} (steps of 2 V) in order to verify the improved repeatability immunity to common mode input. A variable DC voltage source provided an input voltage, filtered to remove noise spectral content greater than 20 Hz, and connected as common-mode voltage to the front-end. For each common mode input value, 50 histograms were built and 50 values of mode were determined. In Fig. 18, the average of 50 sample modes with the experimental standard deviations is depicted for each value of common mode input.

FIG. 18. Mode of WCR for different common mode input voltages with 1- σ error bars.

VII. CONCLUSIONS

The design and the comprehensive metrological characterization of an ultra-low noise acquisition system for fast voltage pulses have been presented. The *CMRR* figure is a critical parameter given the working principle of the presented analogue front-end.¹⁰ Experimental test setups demonstrated a *CMRR* of more than 87 dB in *DC*, consistent with the design expectations. The system showed a 3-sigma low-frequency stability of about ± 0.65 ppm over about 24 h. The temperature coefficient was estimated to be less than 0.1 ppm/ $^{\circ}\text{C}$ in the worst-case condition of fast temperature variations, while humidity dependency was shown to be negligible even for high variations of humidity (from 30% up to 70% of humidity). This is an important result, in fact, such a so robust instrument against temperature fluctuations excludes the need for a water cooling system, by significantly improving the instrument usability. Finally, the worst-case repeatability, the main instrument quality figure, was assessed to be well within the requirements and comfortably immune to common mode voltage inputs.

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