Improving the ATLAS physics potential with the Fast TracKer (FTK) System

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Introduction

• Run II of LHC started - 13 TeV collisions!

• With more than twice the luminosity compared to Run1, average of 40-50 collisions per bunch crossing expected

  • Triggering will become more difficult and time consuming.

• Tracking at trigger level is essential to control rates while maintaining good efficiency for relevant physics processes

  • Helps to resolve complex topologies with $b$- and $\tau$-jets —> Channels involving $b$ and $\tau$ crucial in understanding higgs couplings and in new physics searches

  • Determines the number and position of the primary vertex

  • Improves robustness in jets and missing energy selections in high pileup events

• Critical ingredient for Run2 and beyond

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LHC 8 TeV p-p collision, $\sim 5 \times 10^{33}$ cm$^{-2}$s$^{-1}$ @ 50 ns, $\sim 25$ reconstructed vertexes

Run1 Run2 Run3

PU~40 PU~60
What is FTK?

• FTK is a track trigger, a system of custom electronics (made of ~8000 ASICs and 2000 FPGAs) that does global track reconstruction in the pixel and silicon strip detectors after every level-1 trigger (100 kHz).

• Rapid pattern recognition and track fitting allows global track reconstruction of all tracks with $p_T > 1$ GeV/c to be done in roughly 100 µs, thus providing the tracks at the beginning of High Level trigger (HLT) event processing.

• Software based full tracking in ATLAS Trigger will still be limited to a fraction of the Level-1 triggers

• The inclusion of the FTK processor will fill this gap
FTK Challenges

Tracking has to be very fast - maximum rate of 100 kHz

- Process in parallel: decompose detector data into independent regions (64 Towers)
- Data reduction: each cluster of adjacent pixels/strips defines one “hit"
- Re-bin hit information to coarser resolution → SuperStrips

Several pixels are grouped together into one SuperStrip (SS)
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- Perform tracking in two steps:
  - Find track candidates: Roads
  - Compare fired SuperStrip to predefined track trajectories —> Pattern Matching
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- Perform full-resolution track fitting inside Roads
  - Combinatorics reduced
- Extrapolation to 12 layers
FTK has a custom clustering algorithm, running on FPGAs.

The data are geometrically distributed to the processing units and compared to pre-calculated track patterns.

\[ \chi^2 = \Sigma_i (\Sigma_j A_{ij} \cdot x_j + k_i)^2 \]

Good 8-layer tracks are extrapolated to additional layers, improving the fit.

Pattern matching limited to 8 layers: 3 pixels + 5 SCTs. Hits compared at reduced resolution (Super Strips: SS).

Full hits precision restored in good roads. Fits reduced to scalar products.

\[ p_i = \Sigma_j C_{ij} \cdot x_j + q_i \]
System elements

- **Data Formatter (DF) & Input Mezzanine**
  - find silicon cluster centroids
  - reorganize hits into eta-phi towers

- **Data Organizer (DO)**
  - stores full resolution hits for rapid retrieval within a pattern

- **Associative Memory (AM chip, LAMB, AMB)**
  - pattern recognition in 8 layers

- **Track Fitter (TF) (Auxiliary Card)**
  - linear calculation of chi2, remove duplicate tracks (HW)

- **Second-Stage**
  - find hits in other 4 layers, do 12-layer fit, remove duplicate tracks

- **FLIC**
  - format and send the tracks to the level-2 trigger

- **FTK**
  - 8 full 9U VME crates
  - 5 ATCA shelves
  - ~2000 FPGAs and ~8000 custom AM chips
Data Formatter

- FTK system requires an input interface system to manage:
  - “Clustering” to reduce data volume at the beginning and improve resolution (FTK IM)
  - “Data Formatting” to distribute cluster information to appropriate FTK eta-phi towers

Technical challenges:
- More than 100k hits / event at 100 kHz event rate at PU=80
- Detector as well as readout is not designed for trigger η-φ towers
- Huge number of hits have to be shared among the processors to avoid inefficiency at boundary region

- 32 DF, ATCA boards in 4 crates:
  - each DF connects to 2 towers
- Data are organized in 64 overlapping towers
  - Each tower covers a $\Delta \phi \cdot \Delta \eta \approx 32^\circ \cdot 1.2$
- Board based on a Xilinx Virtex 7 FPGA
  - Large data amount exchanged through a full-mesh backplane
  - Extensive use of high-speed links
FTK Input Mezzanine

Receives 4 inputs links from 2 SCT and 2 Pixel or 2 IBL
100 kHz LVL1 rate with 32 bit 400 words/event (maximum speed of SLINK)

Perform the hit clustering by FPGA
Enough FPGA resources for the complicated pixel clustering

Send the clustered hit data to next board (DF)
Enough data transfer speed for all clustered hit information

Data Formatter delivers hits to the processing units
• Auxiliary Board (AUX):

• Receive silicon hits in 5 Silicon Detector layers and 3 pixel layers from a Data Formatter on 2 QSFP+ fiber blocks.

• Convert each hit into the coarser resolution (superstrip or SS) used in pattern recognition and transmits the superstrips to the AMB on 12 serial links across the VME P3 connector.

• Transmit each hit and the corresponding superstrip to the Data Organizer, (DO) a database that stores the full resolution hits so that all hits associated with a single track pattern can be immediately retrieved.
Associative Memory board

- Aux sends coarse resolution hits (SS) to AM boards.
- AM (using coarse resolution hits) finds the possible tracks the hits can belong to using predefines track maps from simulation.
- SS are received from the AUX and distributed to the AM chip.
  - Chips are distributed in 4 Local AMB (LAMB) mezzanines.
  - In each mezzanine the incoming SSs are then distributed to 16 chips.
  - The same input is distributed to all the 64 chips in parallel through high speed serial links.
- Found roads and match information are distributed back to the AUX.
- I/O through high speed serial links.
- Large computing power.
  - ★ ~3 W for 128 k patterns.
  - ★ one AM06 performing $10^{14}$ parallel comparisons at 16 bits per second.
Associative Memory Chip Design

- The AM chip is a special CAM chip
  - VLSI design using both full custom and standard cells at 65 nm
  - Effort in having low voltage/power device
  - has 10 input links at 2-2.4Gb/s and 1 output link at 2.4 Gb/s
  - AM05 low area prototype 2+1k patterns
  - AM06 large area device submitted this summer ~160mm² and 128k patterns
- The AM identifies the presence of stored patterns in the incoming data
- Input data arrive through 8 independent busses
- Variable resolution patterns: "Don’t care" (DC) feature allows to change the match precision
  - The match precision is set independently for each layer in each pattern
  - Ability to decrease random coincidences while keeping a limited number of patterns
  - Blue: save pattern space by using wider roads
  - Yellow/red: Reduce fake hit combinations by using narrower road in some or all layer
1st stage track fitting (AUX Card)

- Receive on 16 serial links from the AM board the addresses of patterns in which there were hits on the required number of layers (ROAD).
- For each road, carry out the track fitter function:
  - Pass all track candidates within a road through duplicate track removal.
  - Send the accepted track candidates to the Second Stage Board (SSB) on a SFP+ fiber at 6.4 Gbps.

Main processing units 4 Altera Arria V FPGAs. Ability to perform 1 fit in 1 ns in each FPGA.
FTK Second Stage Board

**Main board (SSB Main):** 9U VME board;

**Rear transition module (SSB RTM):** Series of QSFP & SFP+ modules with signals routed to a high-speed connector in the P3 area —> all tested at 6.4 Gbps

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**Each board works with 2 towers:** 4 AUX —> 1 SSB

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**6 FPGAs Xilinx Kintex 7 Series** — large logic use

Large memory for constants and duplicate removal ~900 Gb/s memory bandwidth on board
FLIC

- Receives track data from core crates
- Packs data into the ATLAS ReadOut Driver (ROD) format
- Converts FTK local IDs into standard ATLAS detector module IDs
- Sends data to ReadOut Systems (ROS)
- Performs control, monitoring

- Two input cards (ATCA blade), with each receiving data from 4 core crates via two links per core crate
  - 16 links total for the full system with each for half core crate (one SSB)
- Two output cards (ATCA RTM), each with 8 ReadOut Links to the ReadOut System
- A commercial processor blade for control and monitoring
Integration and Installation Status

USA15 (ATLAS P1):
- Input/Output Fiber installation completed at the end of June in USA 15
- One DF and 4IM in ATLAS partition, processed first data in August
- FLIC output to ROS exercised at full speed

Next Steps:
- Add AUX and output to ReadOut System
- Add AUX+AMB (AM05) and output to ROS
- Add AUX+AMB (AM05)+SSB and output to FLIC-> ROS

One of every board at CERN for full chain tests!
Full chain Integration ongoing: firmware development and data flow debug ongoing

Integration in TDAQ lab

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Integration in TDAQ lab

Installation in the cavern
Conclusion

- The ATLAS Fast TracKer processor will perform track reconstruction in hardware for all Level-1 accepted events (100 Khz)
  - Designed on a combination of ATCA and VME boards, custom and commercial chips
  - TDR: http://cds.cern.ch/record/1602235
  - Full use of tracks will be beneficial for b- or τ-jet identification
- All boards are in final development stage or at the beginning of production
  - Full slice tests ongoing
  - First barrel coverage completion in early 2016 with complete detector volume coverage 6 months later
  - Complete installation will be driven by the luminosity evolution of the machine
- The core technologies used by FTK (AM chips and FPGAs) will play a key role in HL-LHC
  - ATLAS Level 1 Track Trigger upgrade for the HL-LHC is expected to use AM chips for pattern recognition
  - Under consideration the possibility to use an upgraded version of FTK during this period
Backup slides
Pattern recognition

- A pattern consists of a Super-Strip in each layer (10s of pixels/strips wide).
- Uses HEP-specific content addressable memory (CAM) custom chip.
- Patterns determined from full ATLAS simulation.
- Silicon hits seen by $10^9$ pattern simultaneously.
Pattern matching

The FTK basic ideas (1)

**Pattern Recognition**

- The most probable $10^9$ patterns are pre-computed and stored in the Pattern Bank.
  - Pattern matching at limited resolution to reduce the number of required patterns.

- Thanks to the Associative Memory feature all the hits in each event are compared simultaneously with all the patterns in the Bank and track candidates are found.

Pattern recognition is complete when the hits have been transferred off the detector.
New innovation – variable resolution patterns

• Variable resolution: allows different coincidence window in each layer in each pattern

• More effective use of the pattern space:
  - Implementation: don’t care feature to ignore least significant bit of hit

• Blue: save pattern space by using wider roads

• Yellow/red: Reduce fake hit combinations by using narrower road in some or all layer

Equivalent to 5x more patterns
Details on AMChip

AM R&D related FTK

- AMChip03 used for FTK testing
  - 180 nm, 6x12 bit, 40MHz, 1.0 cm², 5K patterns, 1.3W
  - Standard cell
- AMChip04 (2012)
  - 65 nm, 8x15 bit, 100 MHz, 14 mm², 8K patterns, 0.23W
  - Standard and custom cell, Variable resolution
- AMChip05 (2013-2014)
  - 65 nm, 8x16 bit, 100 MHz, MiniAsic (256) and MPW (4k) patterns
  - Serialized I/O at 2 Gbs
- AMChip06 (2014)
  - 65 nm, 8x16 bit, 100 MHz, 1.8 cm², 128K patterns, 3.0W
  - Final version for FTK (8192 chips needed)
AMB specs:

- The expected number of hits for a 70 pile-up WH event is < 650 per layer, or 1 hit per 15 ns. (The 8 layers are handled in parallel.)
  
  – AMB specification is 1 hit per 10 ns.

- The expected rate of roads from the AMB is 8 roads per 10 ns