Development of the Trigger Readout System for the Phase-I Upgrade of the ATLAS Liquid Argon Calorimeters

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The Phase-I Upgrade of Liquid Argon Calorimeter Readout

The LHC upgrade is scheduled to enhance the instantaneous luminosity to $2-3 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ and to provide an integrated luminosity of $\sim 300 \text{ fb}^{-1}$ during Run 3 from 2021 through 2023. The Phase-I upgrade of the trigger readout electronics for the ATLAS Liquid Argon (LAr) Calorimeters will be installed on the ATLAS detector during the second long shutdown of LHC in 2019/2020. The motivation of this upgrade is to provide higher granularity, higher resolution and longitudinal shower shape information from the LAr calorimeters to the Level-1 trigger processors. It will improve the trigger energy resolution and efficiency for selecting electrons, photons, tau leptons, jets, and missing transverse momentum, while enhancing discrimination against pile-up. The readout of the trigger signals will process 34,000 so-called Super Cells at every LHC bunch-crossing at 12-bit precision and a frequency of 40 MHz.

The Super Cells will provide information for each layer of the calorimeter and a finer segmentation in the front and middle layer of the electromagnetic barrel (EMB) and electromagnetic endcap (EMEC). The spatial granularity is thus improved by at least a factor of 4 to 10 compared to the existing Level-1 system. The online calculation of the transverse energy deposited in the Super Cells will provide results close to the energy resolution obtained from the current offline reconstruction.

Architecture of the Upgraded Read-out Electronics

The architecture of the Phase-I trigger read-out is shown in Figure 2. The original functionality of the Front-end Boards (FEBs) is preserved so that the standard read-out of the LAr Calorimeter cells and the legacy trigger system can be operated as before. New Layer Sum Boards (LSB), new base planes and new LAr Trigger Digitizer Boards (LTDB) are added in the upgraded read-out electronics. The LSBs produce finer granularity Super Cell signals in the front and middle layers of the calorimeter. The new base planes will transfer those analog Super Cell signals to the LTDB.

The LTDB is the key electronics board which will digitize the Super Cell signals and send processed data to the back-end electronics, where data are transmitted to the trigger processors. Each LTDB will process up to 320 Super Cell signals. The signals will be digitized by 12-bit ADCs on the LTDB. The output data of an LTDB consists of up to 40 optical fibers, each of which carries the data from 8 ADC channels at 5.12 Gbps through the use of a custom serializer and optical link. With a total of 124 LTDBs in the system, the total rate to the back end electronics is approximately 25 Tbps.

Fig.2 The upgraded LAr trigger readout architecture. The new components are indicated by the red outlines and arrows.

The Phase-I Demonstrator System

Fig.3 Two LTDB versions have been developed with the digital part (BNL) or analog part (LAL/Saclay) on the mother boards. Top left: BNL LTDB; Top right: LAL/Saclay LTDB; Bottom left: back end electronics ABBA; Bottom right: installation of front end electronics.

In order to evaluate technical and performance aspects of the upgraded electronics, a LTDB demonstrator that uses commercial ADCs, FPGAs and optical transceivers has been developed and installed in the recent LHC long shutdown from 2013 to 2015. The demonstrator system, in which about 1/60 of the full new trigger read-out is realized, was installed on the ATLAS detector in summer 2014. The system is comprised of two LTDB demonstrator boards and two ATCA test boards for Baseline Acquisition (ABBA), which serve as digital processing boards and receive the data from the LTDB demonstrators via optical links. In order to verify the proper installation of the demonstrator, calibration data were taken both via the standard readout and with the LTDB.

Fig.4 Noise level of Super Cells in transverse energy. Rapidity dependence of the noise (RMS) in transverse energy for the Super Cells from the LAr Phase I demonstrator in ATLAS. The discontinuity seen at $\eta = 0.8$ is due to a change in sampling ratio and/or electronic gains. The noise level is as expected between 100 and 250 MeV per Super Cell.

Fig.5 Noise level of Super Cells in ADC counts. Rapidity dependence of the noise (RMS) in ADC counts for the Super Cells from the LAr Phase I demonstrator in ATLAS. The discontinuity seen at $\eta = 0.8$ is due to a change in sampling ratio and/or electronic gains. The noise level is well below 1 ADC count and consistent with test bench measurements.

Fig.6 Super Cell pulse shapes for each layer. Responses of four Super Cells from the LAr Phase I demonstrator installed in ATLAS to injected calibration pulses (DAC = 1000 counts to each LAr cell). Size and shape of pulses are as expected and vary due to different detector and electronics properties.

Development of LTDB with Radiation Tolerant Custom ASICs

Fig.7 Test boards for development of LTDB. The final version of the LTDB is being designed with radiation-tolerant ASICs and is planned to be installed on ATLAS detector in the upcoming LHC shutdown. Test boards have been developed to exercise the key components which will be used for LTDB prototype

Fig.8 LTDB Prototype 64 channel test board. The LTDB prototype will implement 80 custom 12-bit ADCs to digitize the Super Cell signals, 20 custom Link-on-Chip (LOCx2) devices to interface with the ADC, prepare the data and serialize them for the optical transmitter, and 20 custom MTx dual channel optical transmitters to transmit the data to the back end. A 1/5 LTDB prototype that will process 64 Super Cell signals has been developed to verify the design and exercise the radiation tolerant custom ASICs.

Fig.9 Block diagram of the full LTDB Prototype.

CONCLUSIONS

The new trigger read-out system for the Phase-I upgrade of the ATLAS LAr Calorimeters is being designed. A demonstrator system has been installed on the ATLAS detector. Preliminary results show that the demonstrator system is functional on the ATLAS detector. With the demonstrator system operating during LHC Run 2, the performance of the new readout system is being measured and experience is obtained for the development and construction of the full trigger readout system for the Phase-I upgrade. Based on the demonstrator system, further prototype boards of the trigger read-out system with radiation-tolerant, custom ASICs are being developed.