The Compact Muon Solenoid Experiment

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Prototypes and system test stands for the Phase1 upgrade of the CMS pixel detector

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Prototypes and system test stands for the Phase 1 upgrade of the CMS pixel detector

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Abstract

The CMS pixel phase-1 upgrade project replaces the current pixel detector with an upgraded system with faster readout electronics during the extended year-end technical stop of 2016/17. New electronics prototypes for the system have been developed, and tests in a realistic environment for a comprehensive evaluation are needed. A full readout test stand with either the same hardware as used in the current CMS pixel detector or the latest prototypes of upgrade electronics has been built. The setup enables the observation and investigation of a jitter increase in the data line as the trigger rate increase. This increase is due to the way in which the clock and trigger distribution is implemented in CMS. A new prototype of the electronics with a PLL based on a voltage controlled quartz crystal oscillator (QPLL), which works as jitter filter, in the clock distribution path was produced. With the test stand, it was confirmed that the jitter increase is not seen with the prototype, and also good performance was confirmed at the expected detector operation temperature (-20°C).

Keywords: LHC, CMS, Pixel detector, Phase-1 upgrade

1. Phase-1 upgrade project of the forward pixel detector

The CMS experiment [1] explores the fundamental laws governing the elementary particles by studying proton-proton collisions at a center-of-mass energy of 13 TeV at the LHC [2] at CERN in Geneva, Switzerland. The innermost part of the CMS detector is a silicon pixel detector which allows for high precision tracking close to the interaction point. The pixel detector covers pseudorapidities up to 2.4 and detects charged particles emerging from beam collisions. It is divided into a barrel pixel detector and a forward pixel detector (FPIX). As the luminosity of the colliding beams is increased to $2 \times 10^{34} \text{cm}^{-2} \text{sec}^{-1}$ in 2017, during the next few years, the readout chips on the present pixel modules would become inefficient, mainly due to buffer overflows. The FPIX detector will be replaced by an upgraded detector with three disks of sensor modules with improved readout chips and faster readout electronics during the extended year-end technical stop of 2016/17 in the “FPIX phase-1 upgrade” project [3].

Prototypes of new electronics have been developed and performance evaluation in an integrated system built with actual components is needed. In addition, the new FPIX detector, assembled at Fermi National Accelerator Laboratory (FNAL), needs to be fully tested and calibrated before it is shipped to CERN.

2. Test stand of full readout chain

The FPIX system is divided into front-end and back-end parts. The front-end consists of pixel sensor modules and readout electronics, and these are mounted in the CMS detector. The back-end system will be housed in a counting room next to the CMS detector cavern and controls the front-end electronics via optical fiber connections.

A test stand of the full readout system was set up at FNAL, using either the same hardware as used in the current CMS pixel detector or the latest prototypes of upgrade electronics. Figure 1 shows the test stand at FNAL, which consists of several sensor modules (in the picture, one module is attached), electronics for their operation, and a VME back-end to control the modules.

The phase-1 upgrade detector system adopts the same scheme in many parts such as electronics control, and clock and trigger distributions, but the new sensor modules transmit digitized data at a rate of 400Mbps while the current modules transmit analog encoded data at 40MHz. In addition, the upgrade system will replace the VME back-end system by a μ TCA system, which is under development. For the purpose of system development, a special add-on board was produced which is mounted on the current VME module for data readout, receives the 400Mbps digitized data, and passes the data to the VME module in the same format as the current system.

The test stand adopts the same data acquisition system as the current detector. Therefore the functionality of prototypes in a realistic environment can be tested and comprehensive evaluation is possible.

Figure 1: Overview of the test stand set up at FNAL. The left part is the front-end side and consists of a sensor module, and control and readout electronics. The right part is the back-end side and the VME modules are for control of the front-end and readout.

3. Jitter issue in the data transfer line

The test stand allows an evaluation of the jitter of the clock distribution system. In an integrated system, it was found that the jitter on the data line increases as the trigger rate increases. Figure 2 (left) shows an eye diagram of the data signal with a random trigger at a rate of 100kHz. The increase is caused by the way in which clock and trigger distribution is implemented in CMS. In CMS the trigger signal is encoded into the Clock-Trigger-Reset (CTR) signal in which a deficit of one rising edge of 40MHz clock signal stands for a trigger signal for the event. The front-end system recovers clock and trigger from the CTR signal using an IC chip based on a phase-locked-loop (PLL), named Tracker-PLL (TPLL). It is found that the jitter arising from the PLL disturbance by missing edges (encoded trigger signals) cannot be ignored in the upgrade FPIX system when data are transferred at a rate of 400Mbps as described in the Section 1.

Figure 3 shows a new prototype of the electronics with a PLL based on a voltage controlled quartz crystal oscillator (QPLL) in the clock distribution path. The quartz frequency is tuned for the LHC operation frequency and a QPLL works as a jitter filter. Two possible configurations of the QPLL position are considered as Figure 4 shows; putting the QPLL in parallel to the TPLL where the QPLL receives the CTR signal directly, or in series to the TPLL where the QPLL receives the clock signal. Figure 2 (right) shows an eye diagram of the data signal with the new prototype (with TPLL/QPLL in series) with a 100kHz random trigger rate. Figure 5 shows the jitter in the clock and data line evaluated with the previous prototype and the new electronics as a function of trigger rate. It was found that both of the new prototypes with the two QPLL/TPLL configurations perform better than the previous prototype, and that the performance is stable with respect to the trigger rate. The jitter of the data line with two optical receivers, namely Zarlink and Fitel (the latter is going to be used in the upgrade detector system) was also measured, and we confirm that the system in total performs stably with respect to the trigger rate.

Assuming the QPLL is adopted, the operation temperature of the electronics is a concern. The quartz oscillator of the QPLL system is guaranteed by the manufacturer to perform down to 0°C, while the upgrade pixel sensor is cooled to -20°C. The electronics board where the oscillator resides is not directly cooled but is located close to the cooling system, and will thus be at a similar temperature. The functionality of the QPLLs on five trial boards were tested in a refrigerator. Figure 6 shows the measured jitter as a function of temperature, relative to the jitter measured at room temperature (20°C). This measurement confirms that the quartz oscillator works at -20°C and even lower, and that the performance is not degraded.

Given the results, a new prototype has been produced, which has a QPLL chip and fits into the detector geometry. The functionality and performance are currently being evaluated.

Figure 2: Eye diagram of the data signal with a random trigger at a rate of 100kHz with a previous prototype electronics in which only a TPLL is used in the clock path (left) and with a new prototype in which a QPLL and a TPLL are set in series (right).

Figure 3: New prototype of electronics with QPLL chip in the clock distribution system

Put TPLL and QPLL in parallel

Put TPLL and QPLL in series

Figure 4: The two layouts of the QPLL and TPLL on the new prototype electronics that were considered.

Figure 5: Random trigger rate dependence of the jitter. The filled symbols show the evaluation of jitter on the clock signal, while the open symbols show the jitter on the data signal.

Figure 6: Temperature dependence of jitter at a random trigger rate of 100kHz relative to the jitter at room temperature. Negative values on the y-axis stand for less jitter.

4. Summary and toward the installation in 2017

We have established a test stand for the full pixel detector readout chain. It has already been used to give valuable feedback for the prototypes produced. The development of the electronics is converging toward the production stage and installation during the extended year-end technical stop of 2016/17. In parallel to this work, this test stand system will be expanded so it can be used to qualify the assembled detector.

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- [2] Lyndon Evans and Philip Bryant, LHC Machine, JINST 3(2008)S08001.
- [3] CMS collaboration, CMS Technical Design Report for the Pixel Detector Upgrade, CERN-LHCC-2012-016.