The new Front-End Electronics for the ATLAS Tile Calorimeter Phase 2 Upgrade

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ABSTRACT: We present the plans, design, and performance results to date for the new front-end electronics being developed for the Phase 2 Upgrade of the ATLAS Tile Calorimeter. The front-end electronics will be replaced to address the increased luminosity at the HL-LHC around 2025, as well as to upgrade to faster, more modern components with higher radiation tolerance. The new electronics will operate dead-timelessly, pushing full data sets from each beam crossing to the data acquisition system that resides off-detector. The new on-detector electronics contains five main parts: the front-end boards that connect directly to the photomultiplier tubes; the Main Boards that digitize the data; the Daughter Boards that collect the data streams and contain the high speed optical communication links for writing data to the data acquisition system; a programmable high voltage control system; and a new low voltage power supply. There are different options for implementing these subcomponents, which will be described. The new system contains new features, including power system redundancy, data collection redundancy, and data transmission redundancy with 2 QSFP optical transceivers, and Kintex-7 FPGAs with firmware enhanced scheme for single event upset mitigation. To date, we have built a Demonstrator - a fully functional prototype of the new system. Performance results and plans are presented.

KEYWORDS: ATLAS; LHC; Tile calorimeter; front-end; FPGA; optical links.
1. Current Tile calorimeter

The Tile Calorimeter (TileCal) is the central hadronic calorimeter of ATLAS, one of the two multi-purpose experiments at the Large Hadron Collider (LHC) at CERN. The calorimeters are crucial components of the ATLAS detector. The electromagnetic lead/liquid argon calorimeter in the central region is enclosed by TileCal and together they provide a precise measurement of hadrons, jets, taus and missing transverse energy. TileCal has a central barrel (divided in 2 partitions) and two extended barrels, for a total of 4 partitions. Each cylinder is composed of 64 modules. TileCal is made of alternating layers of iron plates and scintillating tiles. The tiles are read-out by wave-length shifting (WLS) fibers on both sides of each module. The WLS fibers deliver the light to photomultipliers (PMTs) that are located inside mechanical supports (called drawers) at the outer radius of the iron structure, drawers that also house the front-end electronics. The drawers are configured in pairs as super-drawers. The number of cells is ~5000 and each cell is readout by 2 PMTs. With the present Tilecal readout system, the signals from the PMTs are shaped and amplified in two gains with a gain ratio of 1:64, each signal from either low-gain or high-gain channel is simultaneously digitized with a 10-bit ADC in a rate of 40MHz and stored in the front-end pipeline memory. The analog readout system presents a 16-bit dynamic range to meet the experiment requirements. The analog trigger summation is performed with cells in the same projective tower in order to provide a fast signal for the level-1 (L1) trigger.
2. Requirements and motivation for Upgrade

The upgraded high luminosity LHC (HL-LHC) by ~2025 aims to deliver a luminosity increase by a factor of the order of 5 to 10 relative to the LHC design value \([3]\). The HL-LHC environment presents several challenges for TileCal. The current electronics is ageing and will be submitted to higher radiation levels, so new electronics are needed to guarantee reliability and reduce maintenance costs. Additionally, the increased luminosity will result in higher backgrounds caused by an increased number of minimum bias collisions per bunch crossing, making it difficult for the existing trigger system to reduce the readout rate to manageable levels while keeping the interesting physics events. The digitization of all data is envisaged for an improved trigger with better energy resolution.

3. New electronics design

The current TileCal front-end electronics is based on the 3-in-1 card \([5]\). The signal flow is shown in Fig. 1-top. A 16-bit dynamic range is obtained using two gain ranges and 10-bit ADCs. L1 trigger analog signals (tower sums) are sent over 90m long cables to the off-detector trigger processor. The PMT signals are digitized and buffered in the drawer electronics and later sent off-detector via optical fibres to a ReadOut Driver (ROD) when a trigger is received.

The signal flow for the Phase 2 system is shown in Fig. 1-bottom. These signals are fully digitized and sent off-detector via high-bandwidth optical links to the Tile Preprocessor (TilePPr also known as sROD) \([3]\). With this approach the maximal information is available for the trigger and the signals are much less vulnerable to electronic noise. The TilePPr sends trigger tower signals to the trigger, receives and transmits slow controls (DCS) to the drawer, and establishes the system timing to synchronise the readout stream with the Data Acquisition system. The TilePPr uses Virtex-7 and Kintex-7 FPGAs and Quad Small Form Factor Pluggable (QSFP) optical transceivers.

3.1 Upgrade electronics

The front-end cards process the PMT signals and include drivers for charge injection and Cesium source slow integration calibrations. Three front end alternative strategies are being studied with two of them based on custom ASICs (QIE and FATALIC) and one based on discrete components (3-in-1).

The new 3-in-1 and Mainboard (MB) \([7]\) improve the current design using new discrete commercially available off the shelf components. The 3-in-1 consists of a passive LC shaper with two clamping amplifiers for fast signal processing, and also a slow integrator. The high and low gain amplifiers have a gain ratio of 32. A pair of cables brings the differential signals to the MB for data digitization by a 12-bit 40 Msps ADC, covering a dynamic range of 17 bits. The digitized signals are sent off-detector where they are available for the Level-0 (L0) and Level-1 triggers. The new L0 trigger is based on muon and calorimeter triggers and will provide trigger decisions within a latency of 6 \(\mu s\) \([4]\). The new L1 trigger is based on regions of interest seeded by L0 triggers and on full calorimeter readout.
Figure 1. Signal flow in the current system (top) and in the Phase 2 system (bottom). In Phase 2 the PMT signals are fully digitized and sent off-detector to the TilePPr also known as sROD.

Figure 2. Diagram of the analog front-end readout electronics.

A diagram of the upgraded analog front-end readout electronics is shown in Fig. 2 showing the fast and the slow signal processing chains in which the PMT analog signal is processed in real time. A picture of a MB prototype is shown in Fig. 3-top.

The slow signal integrator monitors the minimum bias current of the PMTs during the collisions. It is also used for the Charge Injection (CIS) and Cesium calibrations [8]. The integrator output is also digitized in the MB.
Each MB is used for the readout of 12 PMTs. Due to the different times of flights, the time of
the signal arrival at the several PMTs is different and the corresponding sampling clock phases of
ADCs need to be adjusted. Altera Cyclone IV FPGAs serve as control and timing units to configure
the front-end boards and to give the sampling clock phase for the ADCs. The FPGAs communicate
with the Daugetherboard via SPI bus to execute configuration commands.

Two other options alternative to the 3-in-1, based on ASICs, are in development. The "Charge
Integrator and Encoder" ASIC (QIE) [9] has no pulse shaping and does the signal digitization using
a 6-bit ADC and 4 gain ranges. The respective signal flow is shown in Fig. 4-left and for a more
detailed description and status see ref. [10].

The "All in One" front-end is based on the Front-end for Atlas TileCAl Integrated Circuit
(FATALIC) ASIC [11], and makes use of the current conveyer concept. A radiation hard ADC
is incorporated into the FATALIC chip, which uses three 12-bit gain ranges (1x, 8x, 64x). The
FATALIC basic circuit is shown in Fig. 4-right and for a more detailed description and status see
ref. [12].

The communication with the back end electronics is controlled by the Daughterboard (DB).
The DB also receives slow control commands from the TilePPr and routes them to the MB or
to the High Voltage (HV) regulation card. Each half DB is controlled by a Kintex-7 FPGA and
there is redundancy in the FPGAs and in the connections with the TilePPr to increase reliability.
The MB sends the digitised signals of the PMTs to the FPGAs on the DB by means of a 400-
pin SAEF connector and the FPGA sends the data to the off-detector electronics by means of
optical fibres. The diagram of the signal flow in the DB is shown in Fig. 5. A modulator based
Figure 5. Diagram of signal flow in the Daughterboard.

QSFP optical module is used to drive the fibres at 9.6 Gbps upload and 4.8 Gbps download speeds.

Commercial optical modulators [13] instead of versatile link driver/receivers have been studied and evaluated for cost effectiveness, small PCB footprint, and the demonstrated radiation hardness of this technology. Modulators also permit the possibility of sending the data at higher rates. Details and status in ref. [14].

3.2 Low Voltage and High Voltage systems

The Low Voltage (LV) system is located at the end of the modules in the outer side of the calorimeter in the so-called fingers [15]. The voltage supplied is +10V and a prototype is shown in Fig. 6 right. The on-detector boards use Point-of-Load regulators (POLs) to supply the needed voltages. To increase system reliability, each MB and DB is functionally separated into halves, each one processing the PMTs from one side of the module. For redundancy, each half has a separate LV feed that could power both halves of a mini-drawer (one mini-drawer is half-long a current drawer) if one feed fails.

For the High Voltage (HV) supply, currently local and remote alternative systems are under study. For the local system, HV from a single feed to the mini-drawer is adjusted for each PMT by a controller card similar to those on the current system. This radiation hard card is housed in the mini-drawers and communicates with slow controls via the DB. A prototype is shown in Fig. 3 bottom. The alternate remote system has the HV distribution off-detector, with 12 HV cables running to each mini-drawer. For details and status of the HV remote system see ref. [16].

4. Demonstrator prototype

The Demonstrator is a hybrid prototype associated to one TileCal module to be integrated into ATLAS for evaluation of the Phase 2 new electronics architecture. It provides digital trigger, but with the addition of backward compatible analog trigger cables to send the analog differential signal to the summing card so that it can be used in the current analog trigger but in Phase 2
Figure 6. (Left) An equipped mini-drawer with 12 PMT blocks with the respective active dividers and front-end boards (inside, not visible). On top there are the Mainboard, Daughterboard and the analog trigger board. The HV board is on the underside (not visible). (Right) Low voltage power supply prototype.

Figure 7. (Left) Phase 2 Demonstrator integrator response to a moving Cesium source for a D6 cell showing peaks corresponding to the positions of the tiles of the cell. (Right) Pulse height versus CIS pulse amplitude.

upgrade this analog trigger will be removed. An equipped mini-drawer is seen in Fig. 6. A TilePPr prototype receives TTC/CANbus commands and sends data to the current ROD. The interfaces are being developed with increased control of configuration, calibration and readout. The detector control system is operational and it uses the legacy control of HV and LVPS with the respective monitoring of voltages, currents and temperatures. A new mobile testbench (Prometeo) is under development [17]. The calibration systems are used routinely to study the performance, examples are shown in Fig. 7. Recent tests of a Demonstrator have obtained performance superior to that of the current system. A CIS scan from the Demonstrator, shown in Fig. 7-right, shows linearity of ~0.05%, an order of magnitude better than the current system [18]. An extensive program of radiation hardness tests has been underway and most of the components in use in the prototypes already fulfill the requirements to stand Phase 2 luminosities.

5. Summary and conclusions

The Tile Calorimeter Phase 2 Upgrade design is well advanced and a Demonstrator module has
been produced. Revision of many components is ongoing to improve performance. Control and
calibration tests are implemented in the Demonstrator that is interfaced with the legacy communi-
cation systems. A test beam has been prepared to take place in October 2015 and again in 2016, and
it is expected that in December 2016 the Demonstrator will be inserted into the ATLAS detector.

Acknowledgments

This work was supported in part by QREN/Compete and FCT, Portugal.

References


