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VICbus: A STANDARD INTER-CRATE BUS

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ABSTRACT

VICbus is a standard inter-crate cable bus being developed by a working group of the ISO/IEC. Derived from an initiative of the VMEbus Working Group of ESONE, VICbus aims to provide users of multi-crate VMEbus and other backplane bus systems with a standard inter-crate connection. Multi-drop operation is provided for up to 31 devices on a cable of maximum 100 metres in length. Two data transfer protocols are specified, compelled (asynchronous) transfers for transparent interconnection of backplane bus systems (VMEbus in the first instance), and high-speed, non-compelled (synchronous) transfers between VICbus interfaces. A limited interrupt mechanism is specified, as well as a simple, but efficient arbitration technique. Conventional technology is employed: copper cables, existing transceivers, and differential signal transmission, together with proven low-level protocols. Data transfer rates in excess of 30 Mbyte/s will be possible on a cable length of 30 metres.

INTRODUCTION

The power and flexibility of backplane bus systems, such as VMEbus, rapidly outgrow the possibilities of a single crate¹ either because it allows insufficient space for the required functionality, or because of the need for redundancy in high reliability systems. With notable exceptions such as Fastbus (IEEE960), the specifiers of backplane bus systems have traditionally not addressed the need for multi-crate systems until well after the standard has matured. Consequently, proprietary inter-crate connections proliferate, and the user suffers from the well known effects of a lack of standardisation: costly and incompatible solutions only partly answering his needs.

The VICbus initiative has its origins in the recognition by a group of VMEbus users, frustrated by the multiplicity of inter-crate connections, that a standard inter-crate bus would bring the same benefits to the system level that the standard backplane bus systems themselves had brought at a

¹ The term "crate" is more or less synonymous with "sub-rack", "card-cage", "chassis" and even "main-frame" and is used to describe the basic enclosure of a backplane bus system, housing backplane(s), card guides, power supplies and cooling.

lower level of modularity. Work began in 1986 within the ESONE² VMEbus Working Group to define the basic functional requirements, and continues under the aegis of an ISO/IEC Joint Technical Committee³.

The general philosophy adopted has been to aim for rapid homologation since the user community has already waited too long for a standard. Consequently, a pragmatic approach has been taken, and no fundamental new concepts are proposed: copper cables, available silicon and proven transmission techniques. In addition, advantage is being taken of the farsighted decision by Creative Electronic Systems SA to place the low-level protocols of their proprietary inter-crate bus, "VMVbus", into the public domain. Work is, therefore, being concentrated on refining and enhancing these protocols, and adding extra functionality. The early submission of the technical proposal to the ISO/IEC should convince any sceptics of the "openness" of the resulting specification.

The name "VICbus"⁴ is an acronym of "VME Inter-Crate Bus", but the specification makes no basic assumptions that prevent its use for connecting backplane bus systems other than VMEbus, combinations of such systems, or even the design of stand-alone devices.

TERMINOLOGY

It is convenient at this point to define some of the terminology pertinent to inter-crate connections, cable buses in general, and VICbus in particular.

Inter-crate connections fall into two categories: backplane extenders and inter-crate buses, both of which may be more or less transparent to the software. Backplane extenders essentially permit the number of devices connected on one backplane to be increased by connecting another crate, with suitable electrical buffering, and allowing more or less of the functionality of the bus to be transmitted to and from the additional crate. Inter-crate buses connect several crates in a multi-drop fashion on a branch, with suitable mechanisms for inter-crate arbitration and addressing, and with provision for the transmission of the backplane bus protocols from crate to crate.

Transparent operation describes the ability of the inter-crate connection to hide its existence. If, apart from some initialisation, which might include the setting-up of address mapping, etc., the user is unaware that transmission of the backplane protocols over the inter-crate connection is taking place, then it has a high degree of transparency. If, however, account of the inter-crate connection must be taken on a cycle-by-cycle

² ESONE: European Standards On Nuclear Electronics committee of European laboratories.

³ International Organisation for Standardisation/International Electrotechnical Commission, Joint Technical Committee 1, Sub-Committee 26 (Microprocessors), Working Group 8.

⁴ The ESONE VMEbus Working Group claims precedence for the term "VIC".

basis, then it is not transparent.

A device is the generic name for either a backplane bus interface, or a stand-alone box connected to an inter-crate bus.

Direct operations on the inter-crate bus are directed to an interface for its internal use, and generate no activity on the associated backplane bus.

A data transfer from a master to several slaves which actively participate in the bus cycle is termed a broadcast, similarly, a data transfer from several actively participating slaves to one master, is termed a broadcastcall. Slave devices which snarf data take no active part in the data transfer protocol, but spy on bus activity and copy the passing data.

In a time-multiplexed environment, it is necessary to differentiate between the physical lines of a bus and the logical signals they carry.

SIGNAL TRANSMISSION

In order to be able to implement VICbus on practical cables, the control signals as well as the address and data, are multiplexed. Differential signal transmission on twisted pair cables is used, with transceivers which allow wired-OR (and wired-AND) logic, permitting both broadcast and broadcastcall data transactions.

A maximum cable length of 100 metres is permitted. However, two sets of timing parameters are specified for cables which are "short" (up to 30 metres) or "long" (up to 100 metres). These different timing values take account of the signal skew caused by distortion due to unequal capacitive loading on the lines, as well as, but to a lesser extent, the dissimilar characteristics of transceiver devices. If the added complication is justified by the increase in performance so obtained, VICbus devices may optimise their internal timing, using the cable length signalled by the state of a line. Where necessary, the timing parameters also take account of "Wired-OR glitch" effects.

Symmetrical, resistive, termination networks at each end of the cable provide the signal voltage reference, and reduce common-mode reflections. The value of the networks is optimised to provide adequate termination for all cables up to the maximum permitted length.

Either flat ribbon or round section cables may be used, provided they can be mated with the specified connector, and meet the required electrical characteristics.

Table I, below, lists the physical VICbus lines and table II, the multiplexed signals.

Table I: VICbus physical lines

NMENONIC	FUNCTION	No. of PAIRS	TYPE
AD31-AD00	Multiplexed address/data	32	Bussed
AP	Arbiter present	1	Bussed
AS	Address strobe	1	Bussed
BBSY	Bus busy	1	Bussed
BG	Bus grant	1	Daisy-chained
BGLOOP	Bus grant loop	1	End-to-end
BR	Bus request	1	Bussed
CLEN	Cable length	1	Bussed
FCN8-FCN0	Multiplexed control	9	Bussed
DEVFAIL	System error	1	Bussed
DS	Data strobe	1	Bussed
IRQSEL1, 0	Interrupt request select	2	Bussed
IRQ7-IRQ0	Interrupt requests	8	Bussed
SERR	Slave error	1	Bussed
SYSRESET	Global reset	1	Bussed
WAIT	Synchronisation	1	Bussed
TOTAL		63	

Table II: Address/data and control signal multiplexing

SIGNAL (ADDRESS PHASE)	LINE	SIGNAL (DATA PHASE)
Address	AD31-AD01	Data
Byte selection	AD00	
Cycle type selection	FCN8	Byte selection
	FCN7	
	FCN6	Read/write
	FCN5	
Device or interrupt number	FCN4	Address qualifier
	FCN3	
	FCN2	
	FCN1	
	FCN0	

DATA TRANSFERS

Since VICbus aims to provide both transparency and the ability to move data rapidly from device to device, two distinct data transfer protocols are specified: "compelled" and "non-compelled". The former is fully handshaken, or asynchronous, and is used to transfer data transparently between backplane bus systems, in which case the timing of the VICbus cycles is interlocked to that of the participating backplane bus systems. The latter is synchronous, the transfers being timed by the data source alone (the master when writing, and the slave when reading) with no handshake, and will typically be used for transfers of data at the highest possible rate between memories located in the VICbus interfaces. In this mode, transparency is not an issue, since no cycles are to be generated on any associated backplane bus. Broadcast and broadcast transactions are possible in compelled cycles, but are precluded in non-compelled transfers, although data may be snarfed.

Table III, below, summarises the specified cycle types and their respective data transfer protocols.

Table III: Cycle types

CYCLE TYPE	PURPOSE	PROTOCOL
Transparent	Crate-to-crate data transfers	Compelled
Transparent (A64)	Crate-to-crate data transfers with 64-bit addresses	Compelled
Direct compelled	Interface-to-interface data transfers	Compelled
Direct non-compelled (1)	Interface-to-interface data transfers	Non-compelled (1)
Direct non-compelled (2)	Interface-to-interface data transfers	Non-compelled (2)
Interrupt acknowledge	Interrupt vector fetch	Compelled

A compelled data transfer cycle is composed of two parts: the address phase, when the multiplexed address/data lines carry address information, and the data phase, when they carry the data. The master uses the address phase to select the slave or slaves with which it intends to exchange data (device number - DN), and the control information to specify the direction of the transfer and the sub-set of the data bus intended to be used (transparent cycles only). In addition, other control signals are used to specify the protocol (compelled or non-compelled), and the function of the subsequent data phase (transparent or direct data, or interrupt acknowledgement). Refer to table II.

The device number field (DN) permits 31 devices to be addressed on a VICbus branch (DN=0 is used to indicate a broadcast or broadcast cycle). However, the transceivers currently available limit the number of connections to 24.

During the data phase, data is moved between the master and the slave or slaves. It may consist of any number of individual transfers in either direction, read or write. Additional address information is transferred on the control lines during the data phase for internal interface register select during direct cycles, and for information specific to the target bus during transparent cycles (e.g. VMEbus address modifiers). Other signals are used to differentiate between direct mode block transfers (where the slave has to increment its internal address pointer) and indivisible read-modify-write cycles. In the case of an interrupt acknowledge cycle, otherwise a normal compelled data read, an interrupter number (IN) is transmitted in the place of the device number, thereby allowing the arbitrary attribution of interrupters (maximum 32) to devices.

The one slave response line (SERR) may be asserted during the data phase to indicate that the data transfer was unsuccessful.

Figure 1 gives a detailed description of a single compelled read transfer.

Two types of non-compelled cycle are specified, NC1 and NC2. NC1 is entirely synchronous and after the address phase (itself always non-compelled), the master writes to the slave(s) at a predetermined rate, with no response expected or given (read transactions are not possible). It is worth noting that the timing of the first data transfer in NC1 has to be slower than those following, to allow time to arbitrate for access to multi-ported memory in typical implementations.

The NC2 protocol is similar to NC1, except that there is an initial compelled data transfer to allow the master to establish the presence of the slave and its ability to proceed with the data transfers, read or write, which it signals by the assertion or otherwise of SERR. Following this initial transaction, data is transferred at a rate dictated by the master if writing (by toggling DS), and the slave if reading (by toggling WAIT). In either case the responses will be pipelined in the cable, and the slave may assert SERR at any time if it detects an error (e.g. parity). The master may check the relationship between DS and WAIT, to ensure that all data have been acknowledged, or to determine at what stage an error was detected.

Figure 1: Single Compelled Read Cycle

Address Phase

- 1) The master asserts the cycle type, device number, address and control signals.
- 2) After the specified set-up time, the master asserts the address strobe (AS).
- 3) All participating slaves assert the synchronising signal WAIT within a specified time.

Data Phase

- 4) The master removes the information from the address/data and control lines a specified time after asserting AS, and continues with the data phase, without waiting for the assertion of WAIT.
- 5) After a set-up time, the master asserts the data strobe (DS).
- 6) The slave fetches the data from the given address, if necessary performing a data cycle on its associated backplane bus, and deasserts WAIT.
- 7) The master latches the data when it receives the deassertion of WAIT.
- 8) The master terminates the cycle by deasserting AS (thus allowing an arbitration cycle to take place).
- 9) The master signals that the bus is free for the next master by deasserting DS.

ARBITRATION

VICbus uses a single-level, daisy-chained, bus request/bus grant arbitration scheme. The inherent redundancy of a distributed, parallel arbitration mechanism à la Fastbus could not be exploited owing to the unacceptable time taken by the arbitration process on a long cable (worst case four bus delays). However, a scheme has been adopted which ensures redundant operation, whilst retaining the speed of the daisy-chained solution, using the principle of a "rotating arbiter". Every device, when it becomes bus master, also assumes the rôle of arbiter, so the arbitration function "rotates", or moves through the system, statistically improving on the worst case arbitration time of twice the end-to-end cable delay (plus logic overheads).

This mechanism also permits redundant operation. The active arbiter asserts a line "arbiter present" (AP), so if the device containing the arbiter fails or is deliberately removed from the VICbus cable, the entire system is able to sense its absence, and a simple time-sliced arbitration process automatically begins to select the new arbiter.

INTERRUPTS

No practical cable bus could hope to implement a fully transparent interrupt mechanism for 31 backplane bus crates such as VMEbus. VICbus compromises by providing a reasonable number of interrupt lines (32), leaving the freedom to the system integrator to assign them to the 31 devices. For the more complex situations, software-based message passing techniques will have to take the place of transparency.

The 32 interrupt request signals (MIRQ) are time multiplexed onto eight physical lines, using the four edges of a 125 kHz, two-phase clock (IRQSEL1, 0). The chosen frequency allows for the worst case 600ns end-to-end propagation time of a 100 metre cable, giving an interrupt latency of 8µs (not counting logic and program delays). Unlike VMEbus, only one interrupter and interrupt handler are allowed per MIRQ to avoid the necessity of another daisy-chain to prioritise the acknowledgments.

The interrupt acknowledge cycle, generated in response to an active MIRQ by an interrupt handler, is an entirely normal, compelled data read, but denoted by a different cycle type number, and carrying an interrupt number rather than a device number. When the requester recognises its interrupt number, it will reply with the appropriate vector information, which it may supply locally or fetch from the originating requester in a backplane bus system. In addition to the vector fetch, an entirely synchronous "look-at-me" use of the MIRQ signals is allowed. A requester may simply assert its MIRQ for a minimum specified time to signal to any device or devices that it requires attention.

UTILITIES

Much effort is going into ensuring fully redundant operation, including "hot" (or live) connection and disconnection of devices to and from the VICbus cable. The aim being that a VICbus branch should be able to resist the failure or deliberate removal of devices during normal operation, without disruption to transactions between third-party devices. The most serious problem encountered so far is the automatic perturbation-free making or breaking of the bus grant daisy-chain. Several possible solutions are under investigation including solid-state relays and active repeaters.

In response to the assertion of the VICbus global reset line (SYSRESET) all devices will perform their internal checks and return to a state where they are available for initialisation. Typically, an interface will provide the options to logically connect the device's local system reset (e.g. VMEbus SYSRESET*) to this line in either direction. In addition, VICbus interfaces may be reset individually, or in groups, by means of single or broadcast direct cycles to the control and status registers.

A device failure line (DEVFAIL) is implemented, the assertion of which allows devices to signal catastrophic failure to the entire system.

To ensure inter-operability of VICbus devices, a mandatory register set is specified. Its functions include selective reset, device status, device capability (synchronous speed, etc.) and a unique manufacturer identification. The basic VICbus mechanism allows a single cycle broadcast status fetch from bit orientated registers (where devices report status on the bit in the 32-bit word corresponding to their device number).

INTERFACING TO BACKPLANE BUSES

The VICbus specification includes (as a "normative" appendix) a minimum set of features for a VICbus to VMEbus interface. In addition, suggestions are made for the implementation of the required basic functionality, including a set of VMEbus register functions. If required, the definitions of VICbus interfaces to other backplane bus systems will be added to the basic specification document in a similar manner.

PERFORMANCE

Transparent (i.e. compelled) cycles on 30 metre cables are subject to an overhead of approximately 220ns, due to the set-up and hold times necessary to account for signal skew, to which must be added twice the cable propagation time (≈ 360 ns). Non-compelled data transfers, which do not have to account for the cable delay, are timed at approximately 120ns/transfer on a 30 metre cable (33 Mbyte/s), and 170ns/transfer on a 100 metre cable (23.5 Mbyte/s).

VICbus STATUS

At the time of writing, two meetings of the ISO/IEC Working Group have been held, with the next scheduled for July 1990. The basic data transfer protocols have been decided, as has the overall functionality of VICbus. Efforts are being made to fully understand the fundamental characteristics of transceivers, cables and connectors, in order that a reasonable and practical choice be made of these essential components. Aspects of redundancy of a VICbus system are also under active consideration, with the aim of achieving perturbation-free, "hot" connection and disconnection.

The Working Group hopes to be able to pass the draft specification to the ISO/IEC Sub-Committee 26 for their official balloting procedure during the course of this year.

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