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A high speed serializer ASIC for ATLAS Liquid Argon calorimeter upgrade

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Abstract

We have been developing a serializer application-specific integrated circuit (ASIC) based on a commercial 0.25-μm silicon-on-sapphire (SOS) CMOS technology for the ATLAS liquid argon calorimeter front-end electronics upgrade. The first prototype, a 5 Gbps 16:1 serializer has been designed, fabricated, and tested in lab environment and in 200 MeV proton beam. The test results indicate that the first prototype meets the design goals. The second prototype, a double-lane, 8 Gbps per lane serializer is under development. The post layout simulation indicates that 8 Gbps is achievable. In this paper we present the design and the test results of the first prototype and the design and status of the second prototype.

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1. Introduction

The optical data links for the ATLAS liquid argon (LAr) calorimeter between the front-end boards (FEBs) and the back-end electronics operate at 1.6 gigabit per second (Gbps) per fiber channel [1-2]. In the LAr calorimeter readout electronics upgrade, it is proposed to remove the Level-1 trigger from FEB and transmit continuously digitized data off the detector. Consequently, the data rate of the optical links increases from 1.6 Gbps to about 100 Gbps per FEB [3-4]. However, the data rate of G-Link [5] or GOL [6] currently used in high energy physics experiments is not more than 1.6 Gbps, too slow for the upgrade.

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Thus for the LAr calorimeter readout electronics upgrade, a high-speed radiation tolerant serializer ASIC is required.

To meet this challenge, we have been developing a serializer application-specific integrated circuit (ASIC) based on a commercial 0.25-μm silicon-on-sapphire (SOS) CMOS technology. The first prototype, a 5-Gbps 16:1 serializer ASIC (dubbed as LOCs1) has been designed, fabricated, and tested in lab environment and in a 200 MeV proton beam. The second prototype, a double-lane, 8 Gbps per lane serializer ASIC (dubbed as LOCs2) is under development. In this paper we present the design and the test results of LOCs1 and the design and status of LOCs2.

2. The design and test of a single-lane serializer

2.1. The design

A 5-Gbps 16:1 serializer, named as LOCs1 [7-8] has been prototyped. LOCs1 is the first step towards optical links for the readout upgrade of the ATLAS LAr calorimeter for the super LHC. The serializer consists of a serializing unit, a phase lock loop (PLL) clock generator and a current-mode-logic (CML) driver, as shown in Fig. 1(a). The serializing unit multiplexes 16-bit parallel low-voltage differential signaling (LVDS) data into a serial bit stream. The serializer unit extends 2:1 multiplexers to a 16:1 one with binary tree architecture. Only the last 2:1 multiplexer needs to work at the highest speed, about 2.5 GHz. With a 312.5 MHz reference clock input, the PLL clock generator provides 2.5 GHz, 1.25 GHz, 625 MHz, and 312.5 MHz clock signals to the serializing unit. The PLL loop bandwidth is programmable to adapt different reference clock qualities. The PLL can be configured to lock to either the rising or falling edge of the reference clock. This edge-selection feature is useful for the users to latch data with optimal timing. The CML driver can drive 50-Ω transmission lines.

The micrograph of the serializer ASIC is shown in Fig. 1(b). The serializer occupies about 50% area of a 3×3 mm² die. All the I/O pins have electrostatic discharge protection except the high speed serial data output pins. The die also includes an LC-tank-based PLL (LCPLL) operating at near 5 GHz. The LCPLL will be used in the next prototype of the serializer array.

Fig. 1. (a) The block diagram of the serializer LOCs1; (b) the die micrograph

The major challenge in the design is to achieve the high speed in the 0.25-μm SOS CMOS technology, which is chosen mainly because of its radiation tolerance. The cut-off frequency of the SOS CMOS technology is higher than that of the bulk CMOS technology with the same feature size, but it is still...
challenging to achieve the speed requirement. The most challenging parts in the design include the voltage control oscillator (VCO), the first stage of divide-by-2 dividers, the last stage of 2:1 multiplexers, and the CML driver. All these parts operate in the highest speed, about 2.5 GHz.

The operating frequency is the key performance of a VCO. The schematic of the VCO is shown in Fig. 2. To boost the operating frequency, an architecture consisting of five-stage multiple-pass-loop ring oscillator [9-10] is chosen. The schematic of each stage is displayed in Fig. 3. Transistors M1, M2, M5 and M6 are constructed as a latch. When the control voltage (Vctrl) increases, the resistances of M3 and M4 reduce, resulting in the increase of the positive feedback gain of the latch. The stronger feedback gain makes the latch harder to switch the output nodes. Thus the stage delay increases and the VCO oscillates at a lower frequency when control node voltage increases. The extra secondary feed forward loop made of transistors M7 and M8 reduces the stage delay in a conventional primary loop made of transistors M5 and M6. Comparing to common differential delay stage, the tail current source is removed to reduce the phase noise due to the up-conversion of the tail transistor low-frequency noise close the oscillation frequency. The oscillating amplitude of this delay stage is rail-to-rail, which also reduces the jitter [11-12].

![Fig. 2. The schematic of the ring oscillator based VCO](image)

The core circuit of a 2:1 multiplexer and a divide-by-2 dividers is a D-flip-flop (DFF), which is required to operate above 2.5 GHz in the last stage multiplexer and the first divider following the VCO. The static transmission gate DFF is chosen because of its speed and good single event upset (SEU) immunity. In the regular DFF, the internal complementary clock signals of the pass gates are generated by inverters. The asymmetric complementary clock signals significantly increase the delay of the pass-gates switching in the DFF and limit the speed of the DFF to no more than 2 GHz. A DFF with symmetrical complementary clock signals is shown in Fig. 4. The DFF can operate over 3 GHz. We use two identical differential-to-single-ended circuits with cross-coupled inputs from a differential VCO delay stage to generate symmetric complementary clock signals. To achieve good immunity from the single-event effects, we use large size transistors and static D-flip-flops in the whole design.
Fig. 3. The schematic of a differential delay stage of the VCO

Fig. 4. The schematic of a static DFF with symmetrical complementary clock signals
The CML driver consists of four stages of CML amplifiers [13], as shown in Fig. 5. Each differential stage has twice the tail current and twice the transistor width of the previous stage. The tail current of the last stage amplifier is 20 mA. The output resistor is 50 Ω to match the impedance of a transmission line.

Fig. 5. The schematic of the CML driver

2.2. Lab test

The test setup is shown in Fig. 6(a). In the laboratory test, a field-programmable gate array (FPGA) based board provided 16-bit parallel data and a clock signal to a dedicated chip carrier board through a twisted pair cable. We measured the high speed serial data parameters through the SMA connectors on board with a high speed real-time oscilloscope or a bit error rate tester. An eye diagram at 5 Gbps is shown in Fig. 6(b).

Fig. 6. (a) Pictures of the test setup; (b) The eye diagram at 5 Gbps
The bit error rates (BER) are better than $10^{-12}$ in the data range from 4.0 to 5.7 Gbps. The average measured parameters of the seven ASICs are listed in Table 1. All parameters are measured at 5 Gbps except the upper and lower working data rate limits.

Table 1. Average values of the measured parameters of seven working boards

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Measured results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Amplitude (peak-peak, V)</td>
<td>1.16</td>
</tr>
<tr>
<td>Rise time (20%−80%, ps)</td>
<td>52.0</td>
</tr>
<tr>
<td>Fall time (20%−80%, ps)</td>
<td>51.9</td>
</tr>
<tr>
<td>Total jitter at BER of $10^{-12}$</td>
<td>61.6</td>
</tr>
<tr>
<td>Random jitter (RMS, ps)</td>
<td>2.6</td>
</tr>
<tr>
<td>Deterministic jitter (peak-peak, ps)</td>
<td>33.4</td>
</tr>
<tr>
<td>Eye opening at BER of $10^{-12}$ (ps)</td>
<td>122</td>
</tr>
<tr>
<td>Power consumption (mW)</td>
<td>463</td>
</tr>
<tr>
<td>Lower working limit (Gbps)</td>
<td>4.0</td>
</tr>
<tr>
<td>Upper working limit (Gbps)</td>
<td>5.7</td>
</tr>
</tbody>
</table>

2.3. Irradiation test

We have performed a radiation test with a 200 MeV proton beam at Indiana University Cyclotron Facility. The test setup is shown in Fig. 7(a). A custom-made BER test system for online error detection was placed in an area shielded by lead bricks. We put two LOCs1 carrier boards in the beam and another one in the shielded area as a reference. To test the possible angle effects, the angle between the beam incident direction and die surface normal was set at 0, 30, 45, or 60 degree during the radiation test. The boards accumulated 90% of the total fluence when their angles were kept at 60 degree. Because the number of the SEUs was small, we did not observe any statistically significant dependence on angles.

The radiation test lasted for 12 hours in the beam and we kept the test system running for 15 hours after the beam off. We did not observe any bit error in the annealing time. We monitored the power supply current of the serializers during the test. The current change is shown in Fig. 7(b). The currents changed less than 6% during the beam time and annealing time. This means the total ionizing dose (TID) effects are negligible for our application. We observed two types of SEUs: single bit errors and synchronization errors. We observed five single bit error events in total which did not affect the link status afterwards. The extrapolated BER for the single bit errors is $1.6\times10^{-18}$ at sLHC ATLAS LAr calorimeter. When a synchronization error event occurred, there were a burst of bit errors in a short duration. After the burst of bit errors, the received data had one bit shift comparing to the generated pseudo-random binary sequence (PRBS) data for error checking in the error detector. The bit shift was removed when the receiver was reset for a word alignment. This burst of bit errors lasted only several tens bits. For each synchronization error event, the link can be recovered on the receiver side without many bit loss. The extrapolated number of synchronization error events is less than three at the ATLAS LAr calorimeter in the whole sLHC life time.
2.4. The LCPLL

An LCPLL [14-15] is also implemented in the same prototype as LOCs1. The LCPLL is the prototype of the high speed and low jitter clock generator for the next generation of serializer ASIC. The block diagram of the PLL is shown in Fig. 8. An LVDS receiver and a CML driver are added as the input and output interfaces. In the block diagram, the PFD is a phase and frequency detector. The charge pump (CP) converts the up and down signals into control current. The low pass filter (LPF) integrates the current into control voltage. The VCO is an LC-tank-based VCO. The divider chain consists of four divide-by-2 dividers, a high speed CML divider and 3 CMOS dividers. Because the bandwidth of the CML driver is not high enough, we monitor the output of the CML divider rather than the output of VCO.

The major difference between the LCPLL and the ring-oscillator–based PLL is the VCO. We choose in the LCPLL an LC-tank-based VCO (LCVCO) because of its high speed, low power, low jitter, and insensitivity to radiation. The schematic of the LCVCO is shown in Fig. 9. Transistors M2 and M3 with their source and drain terminals tied together are used as varactors. Inductors L0 and L1 are on-chip spiral inductors whose Q factors are larger than 21. Transistors M0 and M1 are negative resistance devices to compensate the energy loss of the LC tank consisting of inductors and varactors. Transistors M4, M5, M6, M7 and the resistor R0 form a current reference and transistor M8 is used to mirror the current.
reference into the LC tank. Transistors M9, M10, and M11 form a startup circuit for the current reference. An array of decoupling capacitors (not shown in the figure) is used to reduce noise on voltage reference v1.

![Diagram of the LCVCO]

Fig. 9. The schematic of the LCVCO

The LCPLL has been characterized in laboratory test. Fig. 10 is the waveforms in which the output in yellow locked its phase to the input clock in blue. Random jitter and deterministic jitter are about 1.3 ps and 7.5 ps, respectively. The measured tuning range, from 4.6 to 5.0 GHz, is narrower than the expected one which is from 3.8 to 5.0 GHz. The narrow tuning range issue has been investigated and understood.
The power consumption at the central frequency is 111 mW at 4.9 GHz, comparing to 173 mW at 2.5 GHz of the ring oscillator based PLL used in the 16:1 serializer.

Fig. 10. The waveforms of the PLL output clock (blue) locked to the input clock (yellow)

Two LCPLLs have been tested in a 200 MeV proton beam. The parameters of the irradiated PLLs were measured and compared with those of fresh PLLs. The output amplitude and power dissipation of these PLLs after irradiation increases about 25% and 9% of the average of the PLLs without irradiation, respectively, but the statistic is still very low to draw any conclusions. We will investigate this issue, although as a digital circuit the increase is not significant. There is no significant change in transition times and jitter performances. Both irradiated PLLs are functioning after the test indicating that these PLLs survived the TID test.

3. The design of a double-lane serializer

The second prototype, dubbed as LOCs2, of the serializer ASIC is under development. The second prototype will include double lanes of serializers. The block diagram of LOCs2 is shown in Fig. 11. Each lane has 16-bit LVDS parallel input data and 1 bit CML serial output. The two lanes share one LVDS clock input and an LCPLL. Each serializer operates at about 8 Gbps. Basic architecture and low speed CMOS circuits are inherited from the first prototype.

The design challenge in the new prototype is still to achieve the required high speed. Among all the high speed circuits, the most challenging part is the CML driver. Due to the bandwidth limit of the process we use, a conventional resistor-load CML driver as used in the first prototype cannot achieve the high output amplitude at the required data rate. A similar structure consisting of multi-stage differential CML amplifiers is chosen. The schematic of the CML driver is shown in Fig. 12. Only the last two stages
are shown in the figure. We call the last stage as the main drive stage and call all the stages before the main drive stage as the pre-driver stages. The structure of the main drive stage depends on its load. We choose internal 50-Ω pull-up resistors (R1 and R2) to match the impedance of a transmission line. The switch transistors M7 and M8 are very large, meaning large capacitive loads for the previous stage. To drive this large capacitive load at a high frequency, we have to use multiple stages. In our design, we have five pre-drive stages and one main drive stage. All pre-drive stages have the same structures. Even with multi-stage structure, we still have to use a bandwidth extension technique. We choose the shunt peaking technique [16-17]. Since we cannot afford a pair of embedded spiral inductors (250×250 μm² in the process we use) for each stage, we choose the active shunt peaking technique. Transistors M3 and M4 are used as pull-up resistors. Transistors M1 and M2 operate in the triode region and act as resistors. The equivalent impedance of M3 and M1 is a resistor in series with an inductor. It is true for M4 and M2, too. The equivalent inductance is used to implement the shunt peaking effect. We use an external adjustable voltage (Vctrl) to adjust the peaking strength. Deterministic jitter is simulated in post layout is about 5 ps with 8-Gbps PRBS (2^7-1) signals at the typical process corner and 27 °C.

Fig. 11. The block diagram of LOCs2

The designs of all fast parts in CML logic (orange shapes in Fig. 11) have been done. The LCPLL implemented and tested in the first prototype will be used in the second prototype with small tuning range modification. A bug of the divide-by-2 divider used in the first prototype LCPLL has been identified and a new divider has been designed. The post simulation shows that the maximum operation frequency is larger than 4.2 GHz in the worst case (the slow-slow corner and 85 °C).

The last stage of 2:1 multiplexers and the clock buffer operating at the highest speed have been changed with CML circuits. The clock buffer is used to fan out the high speed clock. The post layout simulation shows that the maximum operation frequency is larger than 5.4 GHz in the worst case (the slow-slow corner, 85 °C). The last stage of 2:1 multiplexer has been changed from the CMOS logic in the
first prototype to the CML logic in the second prototype. Deterministic jitter is simulated in post layout to be about 4.5 ps with 8 Gbps PRBS ($2^{7}-1$) signals (typical corner and 27 °C).

The second prototype will be submitted in the beginning of 2012.

4. Conclusion

To meet the challenge of the ATLAS LAr calorimeter upgrade, we have been developing a serializer ASIC based on a commercial 0.25-μm SOS CMOS technology. The first prototype, a 5 Gbps 16:1 serializer has been designed, fabricated, and tested in lab environment and in 200 MeV proton beam. The test results indicate that the first prototype meets the design goals. The second prototype, a double-lane, 8 Gbps per lane serializer is under development. The post layout simulation indicates that 8 Gbps is achievable.

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References


[8] D Gong, A 16:1 Serializer ASIC for Data Transmission at 5 Gbps, 2010 JINST 5 C12009


[16] Z Gu, A Thiede, R. Tao, CMOS wideband amplifier with an active shunt peaking technique, Joint Symposium on Opto & Microelectronic Devices and Circuits, Wuhan/China, 2004