The LHCb VELO Upgrade

D. Hynds¹, on behalf of the LHCb Collaboration

University of Glasgow, Glasgow, Scotland, UK

Abstract

The LHCb experiment at CERN has recently reached an integrated luminosity of 1 $fb^{-1}$. While the search for new physics continues, preparations for extending the physics goals after the planned period of operation until 2018 are already well underway. The proposed 40MHz upgrade strategy places considerable requirements on the design of new detectors, necessary for the implementation of a fully flexible software trigger. An overview of the current designs for the upgraded vertex detector are presented, including recent R&D and progress towards a first module.

Keywords: LHCb, VELO, Silicon detectors, Pixel detector, Beam telescope, TimePix

1. The LHCb Detector and Upgrade

1.1. LHCb

LHCb [1] is a flavour physics experiment located at the Large Hadron Collider (LHC) at CERN, and is designed to search for new physics via the study of CP violation and other rare physics processes. Due to the correlation of beauty quark pair production in rapidity, the detector is arranged as a forward arm spectrometer, designed to maximise b-quark acceptance. Fig.1 shows the complete layout of the sub-detectors. The vertex detector allows accurate measurement of b-quark decay lengths, while the RICH detectors are used to separate pions and kaons, both dominant decay products in b-physics. Inner and outer tracking regions are used to gain momentum information, with mass resolution provided by the calorimeters. Several alternating layers of iron and detecting elements (MWPC and triple-GEM) distinguish muons from other decays products.

1.2. Motivation for the LHCb Upgrade

The phase 1 goals of LHCb are expected to be completed with the accumulation of 5 $fb^{-1}$. In order to further the scope of rare processes that can be measured, and to investigate or confirm the effects of new physics discovered during the first 5 years of LHC operation, an upgrade of the detector is planned [2]. Since the design luminosity of LHCb is less than that of the general purpose detectors at the LHC, the increase in

¹Email: daniel.hynds@cern.ch
operational luminosity for LHCb does not rely on the upgrade of the LHC accelerator. Presently, defocussing of the beams before the interaction point permits stable running at $1 \times 10^{33} \text{cm}^{-2}\text{s}^{-1}$. The current upgrade strategy proposes an increase of luminosity to $5 \times 10^{33} \text{cm}^{-2}\text{s}^{-1}$ and, more critically, the implementation of a fully software trigger system. As shown in Fig. 2, the trigger yield in several important hadronic channels saturates with increased luminosity, and therefore a more sophisticated triggering is required. This necessitates the replacement of front end electronics throughout the experiment, to enable full detector readout and reconstruction for each bunch crossing.

### 1.3. The Current VELO Detector

Several rigorous requirements were placed on the current vertex detector design [3]. Due to the decay length of b-quarks at the LHC (of the order of 1cm), the distance between the beam and the sensing elements of the detector had to be kept to a minimum, while keeping the total mass of material seen by decay products as low as possible. For this reason it was necessary to place the entire detector in vacuum, and to replace the beam pipe with a thin (300$\mu$m) layer of RF-foil. Due to the operational risks involved with close proximity to the beam, both detector halves were mounted on a mechanical motion system to allow the entire detector to be retracted until stable beams have been reached.

The detector itself is an $n^+\text{-in-}n$ silicon strip detector, with each module formed by two back-to-back sensors; one with strips patterned in the radial direction and the other with strips in the Phi direction. In both the R and Phi sensors, the strip pitch varies with position, between a minimum pitch of 40$\mu$m and a maximum pitch of 100$\mu$m. Two modules are mounted on opposing sides of the beam to form a station perpendicular to the beam axis, with a radial acceptance from $r = 7$mm to $r = 42$mm. Each sensor is read out by 16 front end chips, which are capable of continuous 1 MHz operation (and can read out a maximum of 16 sequential bunch crossings).

### 2. Requirements and Proposals for the VELO Upgrade

#### 2.1. Operation Conditions

The operating conditions of the future VELO fully extend from those of the current detector, and in several areas require full or partial redesign of the existing modules. Where possible it is intended to re-use the existing infrastructure, and as such the proposed detector will have to respect the current limits on
cooling capacity and material budget, ideally reducing the latter. It is intended to continue with the same vacuum chamber and mechanics system, both of which place restrictions on the size and layout of future modules, in addition to the placement of cooling.

The most serious redesign required for the upgrade is the requirement to move to 40MHz continuous readout in order to allow full reconstruction of each event in the online trigger scheme proposed. This will mean the complete replacement of the front end electronics, in addition to changes in granularity which should be imposed to reduce the total occupancy. Radiation tolerance, of both the FE electronics and the sensors, will have to be improved upon, with an expected integrated fluence of $8.5 \times 10^{15} \text{n}_{eq}\text{cm}^{-2}$ at the most inner regions of the detector.

### 2.2. VeloPix, a Pixel Chip VELO

A variation on the current TimePix family of chips [4] has been proposed as a solution for the upgrade. Hybrid chips offer several advantages in particle physics, primarily radiation tolerance and the ability to develop chip functionality and sensor design independently. Tests performed with the current generation of the chip (see below) have proven their ability to perform as a tracking detector for particle physics, and the similar design requirements of the next generation (TimePix3) will provide a test bed for the development of the LHCb chip, dubbed VeloPix. VeloPix will feature an analogue circuitry almost identical to the current proposals for TimePix3, and both will feature data-driven readout over a matrix of $55\mu\text{m} \times 55\mu\text{m}$ pixels.

As indicated above, one of the most critical design issues in the development of VeloPix is the management of data rates and the need for continuous 40MHz readout. For each pixel hit in the chip, the outgoing data stream will need to contain the pixel address (16 bits), time stamp (12 bits) and ADC counts (4 bits). Simulations at a luminosity of $2 \times 10^{34}$ show that the hit rate for the innermost chips will be around 6 particles per bunch crossing, and with an average of 2 hit pixels per particle, this means a raw data output rate of order 15 GBit s$^{-1}$. For this reason, work into various compression schemes has been undertaken. One such proposal is to group information from neighbouring pixels within a $4 \times 4$ region to form a so-called

![Fig. 2. Trigger yields for several physics channels with the current LHCb detector](image)

![Fig. 3. A proposed data reduction scheme for VeloPix](image)
super pixel. In one scheme, shown in Fig. 3, the hits within this region share a time stamp, and the individual pixel addresses are replaced with a 12 bit global address and an indicator of how many hits there were in the super pixel. The individual hit locations then follow, along with their respective TOT values. In scenarios such as this, reductions in bandwidth of up to 30% have been demonstrated, with the gain usually dependent on the average cluster size (the overhead of the super pixel format leads to increased bandwidth for single pixel hits, while providing significant gains for multi-pixel clusters). The restrictions on which compression algorithms will be possible on-chip will come from the FPGA readout boards which receive data from the chips and prepare this to enter the CPU farm for event reconstruction. As the data is pushed off-chip as soon as it is available locally, data from a single bunch crossing will arrive asynchronously to the readout links. Time ordering the output will require significant FPGA resources, and before any clustering can be done in preparation for entry into the event reconstruction the data will have to be unpackaged from any output formats implemented to save bandwidth. The feasibility of online off-detector clustering, and the effect which raw data formats will have on it, is currently under study.

In order to take advantage of the existing cooling interface, a module design has been proposed which retains the current structure (conceptual design shown in Fig. 4). Power dissipation across the module would be roughly constant, with a power budget of up to 3W per chip, and in keeping with the existing detector would sit completely within the secondary beam vacuum. Since this requires that the modules are actively cooled only at the periphery, a high conductivity material must extend until the tip of the modules. CVD diamond has been proposed to fulfil this role, in addition to acting as a mechanical substrate. A 300μm spine of diamond, which can be manufactured with thermal conductivities in excess of 1800 Wm⁻¹K⁻¹, is envisaged, with the VeloPix chips mounted on both sides to ensure complete overlap of the active areas. Metal traces deposited on the diamond surface will route signal lines from the chips to the copper flex cables which will extend from the module edges to the outside of the vacuum hood, following which the data will be converted for transmission via optical fibres to the off-detector readout boards.

An alternative to diamond as a substrate for module construction has also been suggested, based on a silicon wafer with etched micro-channel cooling. Here, two wafers would be bonded together with 50μm wide and × 50μm deep etched channels on the surface of one of them. These channels would then be used to transport the cooling fluid (liquid CO₂) all the way to the edge of the modules. This option would have not only the advantage of cooling power directly under the chips (as opposed to the periphery), but also of perfectly matched coefficients of thermal expansion. Whether or not this technology will be reliable is currently under study in collaboration with other experiments, and the associated risks of working in vacuum must also be evaluated.

2.3. Strip Detector Options

In parallel to developing a pixel-based VELO, work has also been undertaken to consider a strip detector similar in appearance to the current design. Should the data rates for VeloPix exceed what is possible, or the power or material budgets prove to be too tight constraints, then a strip detector could become advantageous. Work has continued in parallel towards the development of a strip detector, presently concentrating on the design of a suitable readout chip and sensor scheme. A prototype of the sensor, to be read out by the current
LHCb strip chip, has been submitted for fabrication, and employs a similar R-Phi pattern to the existing VELO. The strip pitches have been reduced, and more strips introduced, in order to keep a roughly uniform occupancy over the entire detector and to reduce the total occupancy. A readout chip, capable of continuous 40MHz readout and with local clustering implemented is being developed in collaboration with the LHCb silicon tracker group.

2.4. Joint Considerations
In both the strip and pixel options, there are several overlapping areas which can be investigated independently. For the sensor design in particular, decisions such as the sensor thickness and whether to adopt n-in-p or to continue with n+ -in-n can be made before the final adoption of either solution. To this end, analysis on testbeam data with sensors of varying thickness and material type is currently underway. Radiation studies, in particular taking into account the non-uniformity of irradiation in the VELO, will be performed in the coming year.

3. Beam Tests and the Development of the TimePix Telescope

3.1. TimePix as a Tracking Detector
The TimePix chip has been tested extensively in order to determine its suitability for use as a tracking detector for LHCb [5]. In its current form, the chip is a shutter based pixel chip which can operate in 3 distinct modes: Medipix, Time Over Threshold (TOT), and Time Of Arrival (TOA). In medipix mode the on-pixel counter is incremented each time that the charge sensitive amplifier (CSA) output passes threshold, whereas in TOT mode the counter is incremented continuously each clock cycle that the output remains over threshold. As the return to baseline of the CSA is (approximately) linear, the number of clock cycles in TOT mode is directly proportional to the amount of charge deposited in the pixel. The final mode of operation, TOA, begins counting clock cycles from the particle arrival until the end of the shutter, providing timing information for each hit.

The next iteration of the chip to appear, as mentioned above, will be the TimePix3 chip. As stated, this will be much closer in requirements to VeloPix, in particular it will see the shutter based readout of TimePix replaced by a data driven scheme. In addition, while TimePix can only operate in 1 mode per pixel, TimePix3 will give both TOT and timing information simultaneously. A fast hit signal will provide timing information between the particle arrival and the subsequent clock edge, allowing sub clock-cycle timing of around 1.6ns. After the return to baseline of the CSA, each hit will trigger automatic readout, and as the readout time will vary depending on the pixel location along the column bus, these will arrive asynchronously at the output. For the VELO upgrade, the off-detector electronics will have to buffer this data and sort incoming hits into time bins identified by the bunch crossing ID. This will be resource intensive, and require tuning to the latencies of the data readout.

3.2. The TimePix Telescope
In order to fully test the tracking performance of TimePix, it was necessary to construct a telescope with which to measure the single hit resolution. This was done using 9 TimePix planes, 8 in TOT mode and one in TOA. The planes are angled in both x and y to 9°, in order to obtain the optimum resolution (discussed below).

The telescope is read out using an FPGA-based readout, RELAXd [6], developed at NIKHEF. Originally designed as a quad readout for two by two modules, several RELAXd are connected via fan-out PCBs to the telescope planes, one readout board for each half of the 8 TOT planes, and an additional to read out the chip in TOA mode. Crossed scintillators, located at each extremity of the telescope, provide a source of raw triggers which are used to trigger external devices (in some cases after synchronisation, for example to a 40MHz clock for LHC-style detectors), and can additionally be used to monitor and maintain a constant occupancy in the telescope. Once the shutter is open, these triggers can be counted until a fixed number has been reached (to keep occupancy at an acceptable level for pattern recognition), or until a timeout expires. This timeout is used to prevent counter saturation in the TOA plane, which has a depth of order 11k counts.
Since the TOA is a measurement between the particle arrival time and the shutter closing, the shutter length must be less than \(11000 \times T\), where \(T\) is the clock period. This frequency is configurable, from a minimum of around 300kHz to a maximum of 80MHz. The trigger signals and shutter start/stop are also directed to a VME crate which acts as a TDC, allowing more accurate time stamping of tracks.

For external devices under test (DUTs), such as the LHCb beetle chip [7], the TDC enables offline recombination of data. Using in most cases the native output format of the DUT with a linux time stamp (sufficient to match cycles of the SPS), events are constructed using the known times of triggers within each telescope frame.

Each data frame consists of up to a few hundred hits on each telescope plane. Fast nearest-neighbour algorithms have been implemented in the pattern recognition, combined with a linear fit-projection, to construct tracks, which contain a timestamp from the end plane which runs in TOA mode. This rough timestamp can then be matched in time to the TDC recorded by the VME crate, as the TOA granularity is optimised for the raw trigger rate. The track then contains the arrival time of the particle accurate to around 1ns, allowing, for example, phase measurements for analysing data from analogue strip chips.

Improvements in 2011 to the DAQ system of the telescope have allowed track rates of up to 15kHz to be recorded. Simulations using the measured single plane performance have indicated a pointing precision of between 1.5\(\mu\)m and 2.5\(\mu\)m, dependent on the distance between the telescope arms. Using the time resolution of the TDC, timestamped tracks with accuracy of order 1ns are achievable. The TimePix telescope was developed in part under the AIDA project [8], and as such is presented to the community as general infrastructure for detector development. Several detectors have already been integrated into the readout and analysis chain.

3.3. Testbeam Results

Several results from the TimePix testbeams have already been published, both in the characterisation of TimePix as a tracking detector and also on sensors measured in the telescope. The main results of interest for the upgrade are the tracking performance of the chips. Fig. 5 shows a summary of this feature, along with the corresponding data for the current VELO detector. The left hand graph shows the resolution of a TimePix chip with 300\(\mu\)m and 150\(\mu\)m p-in-n sensors respectively, and the optimum resolution is achieved close to the geometric expectation, \(\tan^{-1}(\text{pitch/thickness})\). The right hand graph shows, by comparison, the equivalent data taken with the existing VELO detector with beam during 2010. The resolution is shown for an R-geometry sensor for two different angular spreads and across the complete range of strip pitches.

![Graphs showing testbeam results](image)
4. Conclusions

The LHCb upgrade requires the replacement of all front end electronics throughout the detector and the implementation of a fully flexible software trigger. The implications and restrictions to the vertexing detector have been highlighted, and simulations to better understand the upgrade environment are under way. Two options have been proposed for the VELO upgrade: a pixel detector based on a future version of the TimePix chip, and a strip detector resembling the current VELO. For the pixel detector, highest data rates will force the adoption of some form of on-chip data compression, and the effects of this on the data readout and event reconstruction remain to be simulated. For the strip detector, the larger sensor area will exacerbate the problem of non-uniform irradiation, and will require further study. A readout chip is currently under development, and overlaps the requirements of several sub detectors. Prototype sensors for both options have been submitted for fabrication, and tests on sensor material and thickness are continuing independently of the detector choice. The upgraded VELO is expected to be installed during the planned LHC shutdown in 2018, and is foreseen to operate for the following decade, amassing of the order 50 fb⁻¹.

References