The Compact Muon Solenoid Experiment

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Mailing address: CMS CERN, CH-1211 GENEVA 23, Switzerland

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The phase-1 upgrade of the CMS vertex detector

Mauro Menichelli for the CMS Collaboration

Abstract

The operation of the present pixel detector has started in 2010 with LHC operating at a center of mass (CM) energy of 7 TeV. At the beginning of 2012 the CM energy was increased to 8 TeV and within December 2012 a total of 19 fb^{-1} integrated luminosity has been delivered, with instantaneous peak luminosities approaching $7 \times 10^{33} \text{ cm}^{-2} \text{ s}^{-1}$. The present pixel detector was originally designed for a luminosity of $1 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ and a pileup (number of inelastic interaction per bunch crossing) of 25 for 25 ns bunch spacing. These beam parameters will be reached in the middle of the data taking period 2015-2017 (with an additional increase in the center of mass energy up to the value of 13-14 TeV) and then the peak luminosity will keep increasing until 2017, when it will reach the value of $1.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. The present detector will remain operative until the end of 2016 and will be replaced with an upgraded detector before Long Shutdown 2 (LS2). After LS2 the beam parameters will change again, around 2021 a peak luminosity reaching at least $2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ is foreseen, consequently pile-up will increase up to 50 if the bunch spacing will be kept at 25 ns, or to 100 if the bunch spacing will be brought to 50 ns. In this context the present pixel detector will be unable to perform adequately and this is the reason why a new detector needs to be built and installed before LS2. The new upgraded detector will have higher tracking efficiency and lower mass with four barrel layers and three forward/backward disks to provide a hit pixel coverage up to absolute pseudorapidities of 2.5. The new pixel detector will be described focusing mostly on the barrel detector design, construction and expected performances. Preliminary tests on detector module production will also be presented.

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I. INTRODUCTION

THE operation of the phase-1 CMS pixel detector will start in 2017 when the luminosity will approach $2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ and the average pileup will be in the order of 50 in 25 ns bunch spacing at a center of mass (CM) energy of 13 TeV. With these luminosities tracking efficiency with the current detector, as shown in Fig. 1, would be 80%. For this reason a new detector needs to be built and installed before LS2 [1]. The simulated performance of the upgraded detector for tracking efficiency is also shown in Fig.1. These performances will be achieved with major changes in the readout electronics and in the mechanics. In addition to the problem of data loss (i.e. percentage of lost hits in the tracker) and fake rates induced by the increased luminosity also the issue of radiation damage has played a role in the necessity to build a new pixel tracker.

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M. Menichelli is with the INFN, Sez. di Perugia, Perugia ITALY (telephone: +390755852764, e-mail: mauro.menichelli@pg.infn.it).

When the integrated luminosity will reach the value of 500 fb^{-1} , that corresponds to about $3 \times 10^{15} \text{ neq/cm}^2$, in the first layer of the pixel tracker (1 MGy of total ionizing dose), and about $6 \times 10^{14} \text{ neq/cm}^2$ in the third layer, the charge collection of the pixel sensor (n-doped diffusion oxygenated float zone) will be degraded as shown in Fig.2 [2]. In particular for layer 1 a charge collection of about 25-35% of the original value is foreseen while for layer 3 this charge collection will be 50-60%. Also for this reason a detector replacement is mandatory before reaching 500 fb^{-1} of integrated luminosity.

Fig.1 Tracking efficiency at $2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ as a function of pileup for the present and for the phase-1 upgraded detector.

II. THE GENERAL STRUCTURE OF THE UPGRADED VERTEX DETECTOR

In order to overcome the problems described in section I a new detector has been designed. Although some action will be performed to compensate the reduction of charge collection efficiency due to irradiation, the main problem that will be solved is the reduction in overall tracking efficiency and the increase of the fake rate due to the increased peak luminosity. The new detector layout will be based on 4 layers in the barrel detector (BPIX) compared to the present 3 layers, and 3 layers per side in the endcap detector (FPIX), compared to the present 2 layers. A schematics of the new configuration in comparison with the present configuration is shown in Fig. 3.

Fig.2 Charge collection of the present pixel silicon sensor at various levels of irradiation.

Fig.3 Comparison between the structure of the current detector and the phase-1 upgraded detector. The upgraded detector has 4 barrel layers instead of 3 and 3 endcap disks per side instead of 2.

Although the number of layers has been increased, a big engineering effort has been performed in order to reduce the overall material budget, in particular:

- Removal of electrical/mechanical parts from the interface region between BPIX and FPIX.
- Adoption of a new detector cooling technique based on biphasic CO_2 coolant that uses less material for tubing and a reduced amount of fluid compared with the previously used mono-phase C_6F_{14} .
- A more optimized support mechanics based on Airex foam compound.

For the reduction of data loss a new fully digital ROC (Read Out Chip PSI46DIG) having larger buffers and faster readout speed compared to the previous analog ROC (PSI46V2) has been designed; a comparison between the performance of the two chips is shown in Table I.

Aside the reduced data loss at higher acquisition rate another improvement is the possibility of using a lower signal threshold in order to compensate the reduction in the signal amplitude due to the progressive deterioration of the silicon sensor, caused by radiation damage.

TABLE I
COMPARISON BETWEEN THE PERFORMANCE OF THE ANALOG ROC (PSI46V2) USED IN THE CURRENT PIXEL DETECTOR AND THE NEW DIGITAL ROC (PSI46DIG) USED IN THE UPGRADED DETECTOR

	PSI46V2	PSI46DIG
ROC size	7.9 mm x 9.8 mm	7.9 mm x 10.2 mm
Pixel size	100 μm x 150 μm	100 μm x 150 μm
Smallest radius	4.3cm	2.9cm
Settable DACs / registers	26 / 2	19 / 2
Power Up condition	not defined	default values
pixel charge readout	analog	digitized, 8bit
Readout speed	40 MHz	160 Mbit/s
Time stamp Buffer size	12	24
Data Buffer size	32	80
Output Buffer FIFO	no	yes
Double column Speed	20 MHz	20 MHz (40 MHz)
Metal layers	5	6
Leakage current compensation	yes	no
in-time threshold	3500 e	< 2000 e
PLL	no	yes
Data loss at max Operating flux	$\sim 3.8\%$ at 120 MHz/cm ²	1.6% at 150 MHz/cm ² ($\sim 3\%$ at 580 MHz/cm ²)

III. THE CONSTRUCTION AND QUALIFICATION OF PIXEL DETECTOR MODULES

In this section we will mostly focus on BPIX module construction and qualification, for FPIX modules details can be found in Ref. [1]. Each BPIX module is composed of:

- A flexible cable and connector.
- An HDI (High Density Interconnect circuit) with one or two (in the case of the first layer) TBM (Token Bit Manager, a circuit that handles the readout sequence) onboard.
- A pixel sensor array.
- A digital ROC array (Read-Out Chip).
- Two base strips (replaced by a carbon fiber holder in layer 1).

The pixel sensors have been kept unchanged compared to the previous detector, they have overall lateral dimensions of 16.2 x 64.8 mm², a thickness of $285 \pm 5 \mu\text{m}$ and a pixel size of 100 x 150 μm^2 (for a total of 66560 pixels/sensor) [3]. The modules for layer 1 and 2-4 are shown in Fig. 4.

Fig.4 Layout of the pixel detector modules: a) is for BPIX layers 2-4, it includes (from top to bottom) cable, connector, HDI, silicon sensors, ROCs and base strips, b) module for BPX layer 1, it includes: cable connector, carbon fiber holder, HDI (with 2 TBM), silicon sensor, ROCs.

The construction of a detector module is performed in 4 steps:

- Step 1: bump bonding of the ROC to the sensor,
- Step 2: gluing of base strip (layer 2-4 only),
- Step 3: assembling of the cable connector and fiber holder (layer 1 only) to the HDI,
- Step 4: gluing of the HDI and wire bonding from the ROCs to the HDI and from the HDI to the TBM

Once the module is built, it is tested and calibrated. At the end of this process a grade (A, B or C) is assigned to each module according to criteria that are summarized in Table II; grade A and B modules will be used in the construction of the detector, (grade B modules may be used also as spares) and grade C module will be rejected.

TABLE II
GRADING CRITERIA FOR MODULE TESTING

Criteria	A	B	C
Noise (e-)	< 500	500 ÷ 1000	> 1000
VcalThreshWidth (e-)	< 200	200 ÷ 400	> 400
RelativeGainWidth	< 0.1	0.1 ÷ 0.2	> 0.1
Pedestal Spread (e-)	< 2500	2500 ÷ 5000	> 5000
Bad pixel per ROC	< 41	41 ÷ 167	> 167
Leakage Current @ 150V and 17 °C (uA)	< 2	2 ÷ 10	> 10
Slope (ratio of Leakage current I(150V)/I(100V))	< 2	> 2	-
Ratio (I(150V T=17°)/I(150V T=-20°))	> 20	< 20	-
Efficiency during HRT at 120 MHz/cm ² .	> 98%	95% ÷ 98%	< 95%
Noise (e-) per pixel during HRT	< 600	600 ÷ 900	> 900
Column uniformity problems during HRT	No	No	Yes
Readout uniformity problems during HRT	No	No	Yes

The first qualification test is the thermal and thermo cycle test. During this test, the performance of the module will be tested at the lowest possible temperature of operation in the detector (i.e. -20°C), then, in order to emulate the thermal stress the detector will undergo during its working life, 10 thermal cycles between -25°C and 17°C will be executed, and finally the module will be tested at room temperature (17°C). The diagram for these cycles is shown in Fig.5.

Fig.5 Layout of the thermal cycle test. In the first part the module is tested at -20°C (temperature of operation), then 10 thermal cycles between 17°C and -25°C are performed in order to stress the mechanics and then another complete test is performed at room temperature of +17 °C.

After this thermal test a calibration test is performed using a X-ray tube. The calibration test using X-ray fluorescence lines from various targets (Zinc, Molybdenum, Silver, Tin) is performed to calibrate the detector in the energy range 8.6-25.3 keV. Fig. 6 shows the linearity of the energy measurement in a module.

Fig.6 Measured (in arbitrary Vcal unit) versus expected charge deposit from X-ray fluorescence lines of Zinc, Molybdenum, Silver and Tin in a pixel detector module.

Finally a high rate X-ray test (in direct illumination mode) will measure the efficiency vs. rate of the module in the range from 50 to 150 MHz/cm². Fig.7 shows a high rate test setup with 3 modules under test.

In June 2015 we plan to start the actual production that will continue until March 2016. The final assembly into the mechanical structure should be completed by September-October 2016. The complete tracker will be installed during the winter shutdown that ends in January 2017.

Fig.7 High rate test setup with X-ray tube on top and 3 modules under test.

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