For the upgrade of the ATLAS detector, the innermost stations of the endcaps (Small Wheels, SW) will be replaced.

The New Small Wheel (NSW) will have two chamber technologies, one primarily for the Level-1 trigger function (small-strip Thin Gap Chambers, sTGC) and one primarily dedicated to precision tracking (Micromegas detectors, MM).

Custom front-end Application Specific Integrated Circuits (ASICs) will be used to read and filter information from both the sTGC and the MM detectors.

**Context**

- Current VMM ASIC - advanced analog circuitry
- For operation in ATLAS, data must be stored until a combination of Level-0 and Level-1 triggers selects the data to be sent to the ATLAS DAQ system.
- A window of up to 8 bunch-crossings may need to be read out for a trigger.
- Store hits in the VMM until a Level-0 trigger is received and then select only hits in the bunch crossings of interest for transfer to a companion Read Out Controller (ROC) ASIC.
- The ROC then buffers the events until a Level-1 Accept trigger is received and forwards the relevant data.

**Level-0 de-randomization circuit for VMM**

- The new VMM is a custom 64-channel mixed-mode front-end ASIC intended to be used for both the Micromegas and sTGC chambers of the NSW detector.
- The analog front-end circuitry produces asynchronous data which is digitized and timestamped by a global BCID counter.
- Hit data is held in Latency FIFOs until it is selected by the Level-0 trigger (1 MHz rate, 10μs latency).
- Data is stored in separate channel FIFOs.
- The Level-0 selection circuits examine the data in the queue and decide whether it is copied to the output (if it falls inside a trigger window) or discarded.
- There can be only one data sample per each trigger window, for a given channel.
- Each Level-0 Accept BCID is stored in a separate FIFO, deeper than channel FIFOs, in order to maintain synchronism in case of data overflow.
- The Event Builder reads the data sequentially from the Level-0 BCID FIFO and data FIFOs; in case data FIFOs overflow, only Level-0 BCID is transmitted.

**Read Out Controller**

The Read Out Controller (ROC) ASIC will aggregate, process, and format the data generated by the VMM front-end chips. The ASIC has a flexible architecture designed to optimize the data bandwidth usage for Micromegas and sTGC detectors and for different NSW regions with different hit rates. The ROC will concentrate the Level-0 data streams from up to 8 VMMS, will filter the data based on the Level-1 BCID and transmit the data to FELIX using up to four GBT E-Links, each capable of up to 320 Mbps data transmission.

**VMM CAPTURE**

- Receives data packets from the front-end chip, via a 640 Mbps DDR serial interface.
- The deserializer outputs 10-bit words.
- The data is 8b/10b encoded; data alignment is achieved by detection of “comma” symbols.
- The decoded 8-bit words are assembled into 33-bit words, which are written in the FIFO.

**SROC**

- The subROC reads data from up to 8 VMM Capture modules.
- Extracts the hit data corresponding to Level-1 Events.
- Level-1 trigger has a rate of 400 kHz and up to 60 μs latency.
- Forms packets which are sent to the GBT chip via E-Link.
- Data is 8b/10b encoded.
- Configurable output rate: 320, 160 or 80 Mbps.

**VMMs to read out controller**

- The ASIC for the New Small Wheel, TWEPP 2014.
- The New Small Wheel (NSW) will have two chamber technologies, one primarily for the Level-1 trigger function (small-strip Thin Gap Chambers, sTGC) and one primarily dedicated to precision tracking (Micromegas detectors, MM).

**References**

2. **Gianluigi DE GERONIMO et al., VMM2 - An ASIC for the New Small Wheel, TWEPP 2014**