Electronics Development for the ATLAS Liquid Argon Calorimeter Trigger and Readout for Future LHC Running

Walter Hopkins
University of Oregon
February 18, 2016

On behalf of the ATLAS LAr Calorimeter Group

VCI 2016
Outline

- LAr calorimeter intro
- LHC upgrade schedule
- Phase-I upgrade
- Phase-II upgrade
ATLAS LAr calorimeter intro

- Barrel ECAL (EMB), Endcap ECAL (EMEC), Hadronic endcap (HEC), and forward (FCAL) calorimeter for total of $\sim 180K$ channels
  - Barrel HCAL uses scintillators
- Sampling calorimeter with 4 samplings for a total of $\sim 23$ radiation lengths
- LAr is active material (ionization) with Pb and Cu/W absorber
- Very fine $\eta$ granularity cells in barrel (as small as 0.003125)
Current Liquid Argon calorimeter electronics

- 1524 front-end boards (FEB) handling up to 128 channels
- Signal from cells are given a bi-polar shape (ionization yields triangular shape)
- Many individual ASIC’s on FEB using varying technologies (DMILL BiCMOS, 25 µm CMOS)
- About 60 channels are summed over all layers to form $0.1 \times 0.1$ ($\Delta \eta \times \Delta \phi$) trigger towers
- SCA = analog buffer
- Digitization to readout happens on FEB at 100 kHz trigger rate
LHC upgrade schedule

- Two phase upgrade planned for LHC: Phase-I (2019) and Phase-II (∼2024)
- Detector is radiation hard and doesn’t need replacement
  - Unique challenges for FCAL
- Read-out electronics will need replacement
  - Compatibility with trigger upgrade (to maintain thresholds at high luminosity)
  - Radiation damage
Liquid Argon calorimeter Phase-I upgrade

Current system

Phase-I

- LAr trigger electronics upgrade planned for ~2019
  - Order of magnitude increase in granularity to level 1 trigger
- Level 1 trigger will receive new sums for each layer with higher granularity: supercells
- Allows for new algorithms at L1 (shower shape, layer based thresholds, etc)
- Supercells are digitized at 40 MHz
- Sums are processed by the LAr Digital Processing System (LDPS) and sent to three feature extractors (FEX’s)
  - electron FEX, jet FEX, global FEX

(70 GeV electron deposit shown)
Improvements due to finer granularity trigger objects

- Finer granularity allows better estimation of shower shape
  - Example: $R_\eta = \text{energy ratio between area of } 0.075 \times 0.2 \text{ and } 0.175 \times 0.2$
  - Combo of shower shape variables reduce single electron ($p_T > 20 \text{ GeV}$) trigger rate by 2 with minimal effect on efficiency

- Digital processing on LDPS allows for complex information to be computed
  - Example: layer based noise flags
  - Use only supercells that pass noise flags for $E^\text{miss}_T$ calculation
LAr Trigger Digitizer Board (LTDB) for Phase-I

- 124 LTDB’s for all the LAr systems (EMB, EMEC, HEC, FCAL)
- One board will digitize 312 signals with 12 bits at a 40 MHz rate
- New components developed: dedicated 12-bit hybrid pipeline SAR ADC (130 nm CMOS), transmitter chip for 5.12 Gbps optical link
  - Both radiation tolerant for the whole life-time of ATLAS
- Monitoring of state of board will be available
- Switch from analog cables to optical
- Will be Phase-II compatible

Demonstrator based on COTS

To Tower Builder Board

Walter Hopkins (University of Oregon)
LAr Phase-I Demonstrator

- Demonstrator LTDB that builds supercells installed during the summer of 2014
  - Uses COTS instead of radiation hard component
  - At a test stand and at the detector
- First data taking during LHC Run 2
- Calibration runs have been performed
  - First supercell noise measurements in good agreement with simulated noise

 ATLAS Preliminary
 LAr Demonstrator
 Front layer
 \( \phi = 1.91, \eta = 0.01 \)

DAC = 10000
DAC = 8000
DAC = 6000
DAC = 4000
DAC = 2000

Supercell noise

<table>
<thead>
<tr>
<th>( \eta )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.0</td>
</tr>
<tr>
<td>0.2</td>
</tr>
<tr>
<td>0.4</td>
</tr>
<tr>
<td>0.6</td>
</tr>
<tr>
<td>0.8</td>
</tr>
<tr>
<td>1.0</td>
</tr>
<tr>
<td>1.2</td>
</tr>
<tr>
<td>1.4</td>
</tr>
</tbody>
</table>

RMS in \( E_T \) [MeV]

<table>
<thead>
<tr>
<th>( \eta )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.0</td>
</tr>
<tr>
<td>0.2</td>
</tr>
<tr>
<td>0.4</td>
</tr>
<tr>
<td>0.6</td>
</tr>
<tr>
<td>0.8</td>
</tr>
<tr>
<td>1.0</td>
</tr>
<tr>
<td>1.2</td>
</tr>
<tr>
<td>1.4</td>
</tr>
</tbody>
</table>

- Back layer
- Middle layer
- Front layer
- Presampler

FEBs
Prototype LTDB
Tower Builder Board
FEBs
LAr Digital Processing System (LDPS)

- Digital signal processing on super cells
  - Precise $p_T$ measurement, pile-up subtraction, bunch crossing ID
- Receives digital super cell signals at 25 Tb/s
- Transmits data to level 1 trigger at 41 Tb/s
- 32 ATCA carrier boards, each with 4 AMC cards
- Each AMC contains an ALTERA Aria-10 FPGA
  - Power budget: 80 W per AMC
  - Each FPGA processes up to 312 super cell signals
- Pre-prototype (ABBA) installed in summer 2014
Phase-II upgrade: front-end electronics upgrade

- New two level hardware trigger to cope with increased event pile-up
  - 1\textsuperscript{st} level trigger at 1 MHz shall use LAr Supercell information as input
  - 2\textsuperscript{nd} level trigger at 400 kHz exploits full LAr Calorimeter granularity
- LTDB and LDPS remain unchanged for Phase-II
Front-end upgrade (FEB-2)

- New radiation hard amplifiers, shapers, ADC’s, and optical links
  - Signal is amplified, shaped, and digitized at 40-80 MHz
- 1524 new FEB-2’s processing ∼180K channels
- 16-bit dynamic range per channel is necessary
- No on-detector buffer
- Produces input for LTDB
- 10µs and 60µs latency for L0 (1 MHz output) and L1 (400 KHz output)
- HEC cold pre-amps not replaced

Backend upgrade (LAr Pre-Processor)

- New interface with L0 and L1 trigger
- Digital filters for pileup rejection and calibration (input to L1)
FEB-2 R&D: Shaper and ADC

- Shapers
  - Unipolar vs bipolar: negative lobe of bipolar pulse consumes 1/4 of ADC range but more robust pedestal against pile-up
  - Shaper with programmable peaking being studied
- ADC development: 14 bit radiation hard (0.75 kGy)
  - 14 bit ADC and 2 gains \(\rightarrow\) data for all gains planned to be sent to back-end

Programmable peaking time \(\sim 44, 52, 60\) ns
FEB-2 R&D: front-end on chip, SEE suppression

- Development of pre-amplifier and shaper on one chip
  - BiCMOS 130-180 nm 14-bit Front-end on chip
- Active SEE suppression using redundant signal paths being studied
  - Multiple ADC’s used, if DoutA is too high (compatible with an SEE) use output from DoutB

![Diagram of SEE suppression with redundancy](image-url)
• 60-120 LAr PreProcessor units in ATCA format
• Each has 4 processor FPGA (with at least the performance of Xilinx UltraScale: 120 i/o links)
• Each FPGA will have many links to handle 1 Tb/s
• FPGA’s will either be directly mounted on ATCA boards or on AMC boards
  • R&D is ongoing on the feasibility of directly mounted FPGA’s
  • Direct mounting requires high density Multi-Fiber Push On connectors and good power dissipation
Back-end upgrade: digital filtering

- FPGA’s will perform shaping and digital filtering on each channel
- Calibration of channel energy and signal time (similar but not limited to current Linear Optimal Filtering (LOF) algorithm)
  - This will happen at full calorimeter granularity

Potential pile-up filtering algorithm: extended LOF

- LOF finds signal time ($\tau_c$) and amplitude ($A_c$) by minimizing $\chi^2$
- Extend LOF by also solving for out-of-time pile-up pulse ($A_p$ and $\tau_p$)
- Requires higher sampling rate (80 MHz vs 40 MHz) due to more unknowns

**LOF simulation**

\[ \mu = 200, \eta = 2.34, \text{back layer, 5 samples at 40 MHz} \]

**ELOF simulation**

\[ \mu = 200, \eta = 2.35, \text{back layer, 10 samples at 80 MHz} \]
Summary

• Two-stage electronics upgrade program for LAr calorimeter
  • Phase-I: ~ 2019
  • Phase-II: ~ 2024

Phase-I

• Full prototype boards are being built and tested
• Custom ADC and optical link have been developed
• Factor of 10 increase in level 1 trigger information granularity
• LTDB (digitization of fine granularity info) and LDPS (digital processing) are Phase-II compatible

Phase-II

• Complete system is being re-optimized for high pile-up data taking
  • R&D on shaper, ADC and optical link in 65-130 nm technology ongoing
  • No on-detector buffer
• Back-end upgrade for compatibility with trigger upgrade
  • FPGA’s based calibration and filtering on each channel
  • Digital filtering choice being studied
Calibration boards will be on front-end and inject signal pulses onto calorimeter electrodes
  • Except for on FCAL where signal will go to the FEB-2
Radiation hard ASIC’s being developed
All functionality on one chip
  • Digital-to-Analog converter, pulser switch, logic for channel selection and signal amplitude
Higher currents used to align with new dynamic range
  • Silicon-on-Insulator use foreseen