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The Phase-1 Upgrade of the CMS Pixel Detector

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The Phase-1 Upgrade of the CMS Pixel Detector

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Abstract

The CMS experiment features a pixel detector with three barrel layers and two disks per side, corresponding to an active silicon area of 1 m^2 . The detector delivered high-quality data during LHC Run 1. However, the CMS pixel detector was designed for the nominal instantaneous LHC luminosity of $1 \cdot 10^{34} \text{ cm}^{-2}\text{s}^{-1}$. It is expected that the instantaneous luminosity will increase and reach twice the design value before Long Shutdown 3, scheduled for 2023. Under such conditions, the present readout chip would suffer from data loss due to buffer overflow, leading to significant inefficiencies of up to 16 %. The CMS collaboration is presently constructing a new pixel detector to replace the present device during the winter shutdown 2016/2017. The design of this new detector will be outlined, the construction status summarized and the performance described.

Keywords: CMS Pixel Detector, CMS Phase-1 Upgrade

1. The Phase-1 Upgrade of the CMS Pixel Detector

The CMS experiment [1] at the CERN LHC features as its innermost detector component a hybrid pixel detector. This device comprises a three-layer barrel (BPIX) and two disks on each side of the interaction region (FPIX). A total of 66 million pixels result in about 1 m^2 of active silicon. The sensor polarity is n^+ -in- n and the cell size amounts to $100 \mu\text{m}$ in r - ϕ and $150 \mu\text{m}$ along the beam direction¹. The detector has been taking physics data since 2010. In 2015 the good-channel fraction was 98.6 %, while the uptime (in runs with the magnet on) was 98.7 %. The hit efficiency is high, above 99 % for all layers, and the resolution is excellent. For example, during 2015 a resolution of $10.6 \mu\text{m}$ was observed in r - ϕ for barrel layer 2.

The present CMS pixel detector was designed and built for the design instantaneous LHC luminosity of $1 \cdot 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ and a bunch spacing of 25 ns. It is expected that the LHC instantaneous luminosity will reach around $2 \cdot 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ during the next couple of years, allowing 300-500 fb^{-1} of data to be collected before Long Shutdown 3 (which will start around 2023). At a bunch spacing of 25 ns this leads to 50 simultaneous proton-proton collisions per bunch crossing (pile-up) and hit rates of up to 600 MHz/cm^2 in the innermost pixel barrel layer. Under such conditions the present pixel detector would suffer from a hit inefficiency of 16 % in the innermost barrel layer, mainly due to buffer overflow in the readout chip (ROC). In combination with the relatively low redundancy the impact

on tracking efficiency and fake rate would be substantial. The Phase-1 upgrade of the pixel detector will recover the hit and tracking efficiency. At the same time the Phase-1 upgrade will result in a reduction in the material budget of the pixel detector. In particular in the forward tracking volume, $1.2 < |\eta| < 2.5$, a substantial reduction will be achieved.

2. The Detector Concept

The Phase-1 pixel detector [2] will be installed in the CMS detector during the extended winter technical stop 2016/17. The relatively short time available, both for detector R & D and construction, as well as for commissioning of the detector once it has been installed, has driven the concept of an “evolutionary upgrade”, with hopefully minimal impact on data taking. In particular, the sensor technology, pixel size and overall module concept remain unchanged.

The most important changes can be summarized as follows:

- A new, improved readout chip will recover the hit efficiency.
- An additional fourth barrel layer and third disk (per side) allows 4-hit coverage over the full detector acceptance. This leads to more robust tracking and track seeding.
- The innermost barrel layer was moved closer to the beam line, from 4.4 cm radius to 2.9 cm. This improves the vertex resolution and b-tagging efficiency.
- The amount of material is reduced by moving to an evaporative CO_2 cooling system, relocating electronics boards to higher pseudorapidity values and using a lighter mechanical support structure.

A comparison between the present layout and the Phase-1 layout is shown in Fig. 1.

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¹CMS uses a right-handed coordinate system, with the origin at the nominal interaction point, the x -axis pointing to the centre of the LHC ring, the y -axis pointing up, and the z -axis along the anticlockwise-beam direction. Cylindrical coordinates (r, ϕ) are used in the transverse plane, ϕ being the azimuthal angle around the z -axis. The polar angle θ is measured from the positive z -axis. The pseudorapidity η is defined as $-\ln[\tan(\theta/2)]$.

Figure 1: Layout of the present (bottom) and upgraded (top) pixel detector, in r - z view.

3. The Phase-1 Pixel Readout Chip

The readout chip is based on the present psi46 ROC [3]. In particular, it uses the same $0.25\,\mu\text{m}$ CMOS technology and zero-suppressed readout, as well as being based on the column drain architecture. The chip comprises 80 rows and 26 double columns. To increase the bandwidth, the 40 MHz analogue readout has been changed to 160 Mbit/s digital readout, requiring the addition of an 8 bit ADC. The buffer depths of the hit and time-stamp buffers were increased from 32 to 80 and from 12 to 24, respectively. Furthermore an additional readout buffer has been added. The chip-internal cross-talk was reduced and the comparator improved, leading to a reduction of the threshold from about 3200 electrons to about 2000 electrons. This increases the efficiency, as smaller clusters can be identified. The spatial resolution and detector longevity are improved as well.

The standard version of the chip will be used for barrel layers 2-4 and FPIX. It has been tested in beam tests, where it ran stably with a threshold as low as 1800 electrons [4]. The chip was also tested after irradiation with 23 MeV protons to doses of 0.6 MGy and 1.2 MGy, corresponding to the doses expected in layer 2 and 1 after $500\,\text{fb}^{-1}$ respectively [5]. Also higher doses of 2.4 and 4.8 MGy have been tested. It was possible to trim the chip to a threshold of below 1900 electrons, with a noise of less than 180 electrons, for all doses. The hit efficiency was measured versus hit rate and for the two realistic dose levels no degradation was observed for layer 2 hit rates.

Both simulations and measurements show that the inefficiency for layer 2 hit rates is below 2 %, but for the expected hit rates in layer 1, the predicted inefficiency would still be too high. This was expected and a dedicated version of the chip for the innermost barrel layer has been developed. This chip will feature the readout of groups of 2×2 pixels. The first version of this chip has recently been delivered from the foundry, and testing has started. A second submission is being prepared.

4. The Phase-1 Pixel Modules

Figure 2 shows exploded views of the Phase-1 pixel modules. The n^+ -in- n pixel sensor has an active area of $16.2 \times 64.8\,\text{mm}^2$ and comprises 66 560 pixels. The sensor is bump-bonded to 16 ROCs, which are thinned down to about $180\,\mu\text{m}$ for layers 2-4, while thinning to $75\,\mu\text{m}$ is foreseen for layer 1. A very thin

Figure 2: Exploded views of the pixel modules for barrel layers 2-4 (left) and barrel layer 1 (right). From top to bottom the following components are shown: cable, HDI, sensor, ROCs and, for layer 2-4 modules only, base strips.

PCB, the High Density Interconnect (HDI), is glued on top of the sensor. It distributes low and high voltages as well as clock and trigger signals, and routes the data to one (layers 2-4) or two (layer 1) Token Bit Manager (TBM) ASIC(s). The TBM organizes the readout and aggregates and formats the data. The data are shipped off the module in 1, 2 or 4 data streams of 400 Mb/s, where the number depends on the layer. The connection to the power and readout boards is realized with a 1 m long low-mass micro twisted-pair cable. The layer 2-4 modules are glued to $250\,\mu\text{m}$ thick support strips (“base strips”) made of Si_3N_4 , which allow the modules to be screwed to the support structures. For layer 1 modules carbon fiber clips at the short sides of the modules are used instead, which brings the material budget of layer 1 modules down to 0.74 % of a radiation length. The FPIX modules differ in some details (e.g. the cable), but use the same rectangular geometry. This represents a simplification with respect to the present detector, where several wedge-shaped detector geometries were used for FPIX. In total 1 856 modules, comprising 124 million channels, are required. The production of the pixel modules is realized in a distributed scheme, with a number of different consortia, each responsible for the production of a certain part of the detector (e.g. a layer). The module construction procedure differs somewhat from centre to centre, but the typical procedure is described below. The sensors are produced in industry, including the placement of the Under-Bump Metallization (UBM). The ROC wafers are also produced in industry, and the ROCs are tested after reception by CMS. The ROC wafers are then sent to another company that places the UBM and the solder balls, and performs the thinning and dicing of the wafers. The bump-bonding (flip-chipping and reflow) takes place either in industry or is performed in-house. The sensor-ROC package is called a bare module. The bare module is tested, either before or after reflow, and faulty ROCs are removed and replaced. In the next step the HDI, to which the TBM has already been glued and wire-bonded, and the base strips are glued to the bare module, using manually operated but

Figure 3: Number of pixel defects per module (left) and hit efficiency scaled to 120 MHz/cm² per ROC (right). In the legends, N corresponds to the number of entries, μ and σ are the mean and RMS, and "< / >" gives the number of under- and overflow entries. The dark and light histograms represent the detector-grade and rejected modules, respectively.

precisely aligned z -stages. This is followed by wire-bonding of the HDI to the ROCs.

For module qualification, the same test procedure is followed by all BPIX centres, using identical data analysis software, the same grading criteria and a common database. During cold qualification the modules are mechanically stressed through ten thermal cycles between +17°C and -25°C. An electrical test is performed at -20°C (which is the nominal temperature for operation in CMS), both before and after the cycling, as well as at room temperature after warm-up. In addition, the current-voltage characteristic (IV-curve) is measured at both temperatures. Grading is mainly based on the number of defective (dead or noisy) pixels and the leakage current behaviour.

Each module is tested under X-rays. The most important test is the measurement of the performance under X-ray rates of 50 and 150 MHz/cm². Grading is based on the hit efficiency (measured with calibration pulses), the noise, and other variables. In a second test an energy calibration is performed, using X-ray fluorescence from four different targets. Since the energy levels are known, this allows the ROC response to be calibrated in electrons.

In the following the status of BPIX module production as of February 2016 is summarized. In total 889 detector-quality bare modules have been built. Thus far, the yield for bare module production is 89.9 %. From these, 499 detector-grade full modules have so far been constructed, which corresponds to about 40 % of the required quantity (including spares). The quality of the accepted modules is excellent. Figure 3 shows preliminary results from the modules so far produced, namely the number of pixel defects per module, which has a mean of only 0.4 per mille, and the measured hit efficiency scaled to the layer 2 hit rate. Module production will continue until May 2016.

5. Detector Mechanics

BPIX Mechanical Support Structure. The BPIX modules are screwed or clamped onto support strips, so-called facettes (Fig. 4), made out of high thermal conductivity carbon fiber

Figure 4: CAD model of the BPIX detector support structure, showing four layers of facettes, supported by end flanges. The cooling pipes are also depicted.

Figure 5: CAD model of the BPIX supply tube. The interaction point is to the left. The most important components visible are, from left to right: module cables (pink), Opto-Hybrids (grey), DC-DC converters (green/yellow).

(CF) composite material (K13D2U). The material of the facettes is minimized through rectangular cut-outs. The facettes are glued onto the cooling pipes, which are embedded into grooves in the CF. The facettes are supported by end flanges (one per layer). These end flanges are made out of a light-weight sandwich of CF/Airex foam/CF, except for the layer 4 end flange. This one carries the weight of the detector and is therefore made out of CF composite material only. The construction of the support structure is ongoing and module mounting is expected to start in April.

BPIX Supply Tube. The supply tube (Fig. 5) is a support structure (built in half-shells) of 2.4 m length. It carries about 15 types of electronics boards for power distribution and readout, and supports the services, i.e. cooling pipes, optical fibers, and module cables. Also active components such as Opto-Hybrids for electro-optical conversion as well as DC-DC converters are located here. The components are arranged in a complex stack. The supply tube is made out of CF plates (close to the interaction point (IP)) and CF skins covering an Airex foam filler (further away from the IP). Shielding foils are placed both inside and outside of the supply tubes. The end flanges are made of Aluminium and glass-fiber reinforced plastic. The production of the supply tubes is progressing well.

Figure 6: CAD model of an FPIX half disk.

FPIX Disks and Service Cylinder. FPIX follows a similar concept, with services, DC-DC converters, Opto-Hybrids and auxiliary PCBs installed inside half-shell CF support structures, known as service cylinders. The pixel modules are arranged in half-disks as two concentric rings (Fig. 6). The half-disks are also located inside the service cylinders. The modules are glued with thermal film onto support “blades” made of Thermal Pyrolytic Graphite (TPG). The blades are themselves glued into graphite rings. The cooling tubes are embedded in these rings, and the ring surface is closed with a CF skin. Good thermal contact between the blades and rings is crucial. All disks and half cylinders have been prepared and the next step is the cooling tube installation.

6. Services

Evaporative CO₂ Cooling System. While the present pixel detector is cooled through a mono-phase cooling system with the coolant C₆F₁₄, the Phase-I detector will be cooled via a bi-phase CO₂ cooling system, operated at a nominal temperature of -20°C . This will lead to more effective cooling, as the latent heat of the coolant is exploited to remove the heat, and will allow the material of the cooling system to be reduced, as the high vapour pressure of CO₂ allows the usage of thin pipes. On the BPIX layers, stainless steel pipes with an inner diameter of 1.7 mm and a wall thickness of $50\mu\text{m}$ are used. The loops are several metres long and remove heat loads of typically 200 W. The routing is complex, starting on the supply tubes, where DC-DC converters and Opto-Hybrids are used to pre-heat the CO₂ (i.e. to bring it close to the boiling point). Extensive studies of the pipe bending and laser welding are ongoing.

DC-DC Conversion Power System. The new pixel detector features 1.9 times the number of readout channels compared to the present detector, resulting in a factor of almost four higher losses on the 50 m long low voltage supply cables. In order to power the detector with the existing power supplies and cables, a DC-DC conversion powering scheme is employed for both BPIX and FPIX [6]. The DC-DC converters are installed on the service structures, at distances of 1-2 m from the pixel modules, at $|\eta| \approx 4$. They receive an input voltage of 10 V and deliver voltages of 2.4 V and 3.3/3.5 V to the pixel modules. The DC-DC modules are a custom development, based on the

FEAST2 ASIC. The size of the PCBs amounts to $2.8 \times 1.7\text{ cm}^2$ and the weight of one module is about 3 g. The performance is excellent, with a power efficiency of above 80 %. A total of 1 184 DC-DC converters will be installed. The production of the DC-DC converters is finished.

7. System Test and Pilot System

System tests are performed with the goal of exercising the complete optical readout chain with final back-end electronics, the complete power chain and the CO₂ cooling system. One example is the measurement of the pixel module noise (extracted as the width of so-called S-curves) when the module is operated through the full final power chain, including the power supply, cables, DC-DC converters and supply tube power boards. A total of 26 DC-DC converters were operated with nominal loads. No significant increase of the noise, compared to conventional powering through a test board, was observed.

During Long Shutdown 1 (2013/14) eight prototype Phase-1 pixel modules were installed in the CMS detector, on the third, so far unpopulated disk. Half of these modules are powered conventionally, half via prototype DC-DC converters. This so-called pilot system was taking data in 2015 and will continue to do so in 2016. The motivation of this effort is to gain operation experience under realistic conditions, which will hopefully lead to faster and more efficient commissioning of the whole detector in 2017. In 2015 the system was commissioned and integrated into the central DAQ and control system. While only limited data taking was possible so far, during commissioning a problem with the jitter on the clock line being too large was detected. The problem was cured by adding QPLL chips.

8. Summary

The CMS Collaboration will replace its pixel detector in the extended winter shutdown 2016/2017, to maintain the excellent performance of the pixel detector under more challenging running conditions. Module production is in full swing, and all tests so far, including beam and irradiation tests, have revealed excellent module performance. The mounting of modules onto the support structures will start soon, followed by commissioning of ever larger fractions of the detector.

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