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Upgrades of the CMS Outer Tracker detector for the HL-LHC

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The LHC machine is planning an upgrade program which will smoothly bring the luminosity to about $5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ around 2028, to possibly reach an integrated luminosity of 3000 fb^{-1} in the following decade. This High Luminosity LHC scenario, HL-LHC, will require a preparation program of the LHC detectors known as Phase-2 upgrade. The current CMS Outer Tracker, already running close to its design limits, will not be able to survive HL-LHC radiation conditions and CMS will need a completely new device, in order to fully exploit the highly demanding operating conditions and the delivered luminosity. The new Tracker should have also L1 trigger capabilities. To achieve such goals, R&D activities are ongoing to explore options and develop solutions that would allow including tracking information at Level-1. The design choices for the CMS Outer Tracker upgrades are discussed along with some highlights of the R&D activities.

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Upgrades of the CMS Outer Tracker for HL-LHC

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Abstract

The LHC machine is planning an upgrade program which will smoothly bring the luminosity to about $5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ around 2028, to possibly reach an integrated luminosity of 3000 fb^{-1} in the following decade. This High Luminosity LHC scenario, HL-LHC, will require a preparation program of the LHC detectors known as Phase-2 upgrade. The current CMS Outer Tracker, already running close to its design limits, will not be able to survive HL-LHC radiation conditions and CMS will need a completely new device, in order to fully exploit the highly demanding operating conditions and the delivered luminosity. The new Tracker should have also L1 trigger capabilities. To achieve such goals, R&D activities are ongoing to explore options and develop solutions that would allow including tracking information at Level-1. The design choices for the CMS Outer Tracker upgrades are discussed along with some highlights of the R&D activities.

Keywords: HL-LHC, Tracker, Silicon detector

1. Introduction and motivations

The present CMS Outer Tracker [1] was designed to operate without any loss of efficiency up to an integrated luminosity of 500 fb^{-1} and an average pile-up (PU) of less than 50 collisions per bunch crossing.

During the High Luminosity phase of the LHC (HL-LHC), expected after 2028, the instantaneous luminosity will reach and then exceed $5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ with the aim of collecting 3000 fb^{-1} of integrated luminosity in ten years. The present Outer Tracker and Phase-1 Pixel detector [2], which will be installed at the end of 2016, would be unable to cope with even the first few years of operation of the HL-LHC and will therefore need to be replaced during the long shutdown (LS3) needed to install the machine components for the LHC upgrade.

The current Tracker will not be compliant with the significantly higher rate and longer latency of the upgraded trigger system that is crucial for operation at high luminosity [3]. Moreover the increase of leakage current in the Outer Tracker sensors due to irradiation will be fatal and almost all the double-sided modules will be no longer operational already after 1000 fb^{-1} at the achievable minimum coolant temperature of -20°C , as shown in Fig. 1. The loss of hits on many layers of the Tracker results in a degradation of track reconstruction performance with reduced efficiency and increased fraction of ghost tracks² significant enough to have an unacceptable impact on the physics programme of CMS.

Despite the foreseen improvements, the muon and calorimeter-based lowest level trigger (*Level-1* or *L1*) will

Figure 1: Map of non-functional modules (in blue) after the accumulation of an integrated luminosity of 1000 fb^{-1} , for the achievable minimum coolant temperature of -20°C [1, 3].

not be able to withstand the L1 trigger rate due to ghosts generated by the PU and the limited resolution: e.g., in the muon case, no transverse momentum (p_t) threshold is sufficiently effective in reducing the rate. The Tracker is then required to provide high- p_t tracks to the L1 system. Due to the increased L1 complexity the foreseen latency will be increased.

The main requirements for the Outer Tracker upgrade [3] can be summarized as follows:

- radiation tolerance and cold (-20°C) operation to make the Outer Tracker functional up to 3000 fb^{-1} .
- Increased granularity and optimized layout to keep the occupancy below $O(1\%)$ up to PU of 140 events (possibly a PU of 200 events) and to achieve a robust pattern recognition.
- Track trigger capabilities to contribute to the L1 trigger.
- Large readout bandwidth and deep front-end buffers to comply with the higher rate (750kHz) and the long latency

¹On behalf of CMS Collaboration.

²A ghost track is a reconstructed track not unambiguously associated to a simulated track. The fraction of ghost tracks is estimated with Monte Carlo simulation.

Figure 2: The concept of the low- p_t hit rejection in closely-spaced sensors where the “selection window” defines an accepted “stub”.

(12.5 μ s) of the upgraded L1 trigger system.

- Minimization and optimization of the passive material to reduce multiple scattering, nuclear interactions, bremsstrahlung and photon conversions.

2. Modules and layout

The key L1 functionality of the upgraded Tracker, extensively described in [3, 4], is based on data reduction performed on the so-called p_t -modules [5]. The p_t -modules are composed of two closely-spaced silicon sensors read out by common front-end ASICs capable of correlating the hits from the two sensors, as sketched in Fig. 2; thanks to the strong magnetic field, hit pairs that form “stubs” compatible with particles above the chosen p_t threshold are selected and dispatched to the L1 trigger system at every bunch crossing. All other hits are stored in the front-end pipelines waiting to be read out when a trigger is received. A uniform p_t threshold throughout the tracking volume is achieved by tuning the acceptance window, programmable in the ASICs, and by choosing different sensor spacings across the Tracker regions.

Two types of p_t -modules, shown in Fig. 3, are under development. “2S” modules are composed of two strip sensors each approximately $10 \times 10 \text{ cm}^2$ in area, with two rows of $\sim 5 \text{ cm}$ AC-coupled strips with $90 \mu\text{m}$ pitch. The sensors are mounted such that the strips of the two sensors are parallel to each other. They will be used in the outer regions outside a radius of approximately 60 cm (in red in Fig. 4 and 5). “PS” modules are composed of two sensors each approximately $5 \times 10 \text{ cm}^2$ in area, one segmented into approximately 2.5 cm AC-coupled strips with $100 \mu\text{m}$ pitch, and the other segmented into DC-coupled “macro-pixels” of size $100 \mu\text{m} \times 1.5 \text{ mm}$. PS modules are de-

Figure 3: Three-dimensional view of the assembled 2S module (left) and of the PS module (right).

Figure 4: One quarter of the standard layout option. Blue lines correspond to PS modules, red lines to 2S modules. The Pixel detector with forward extension [3, 11] is shown in green.

Figure 5: One quarter of the *tilted* layout option. Refer also to caption of Fig. 4.

played in the radial range between 20 cm and 60 cm, i.e. the inner region (blue in Fig. 4 and 5). The macro-pixels precise measurements of the z coordinate is crucial for primary vertex discrimination at L1 and for a robust pattern recognition. In both cases the sensors are connected to the readout hybrid and to the auxiliary electronics for powering and readout, all of which is integrated into the module assembly. One (2S module) or two (PS modules) “service hybrids” carry a 5 Gb/s data link, an optical converter, and the DC/DC converter that provides power to the module electronics.

The sensitive elements of the modules are planar silicon sensors, which will be exposed to particle fluences up to $1.5 \cdot 10^{15} \text{ neq} \cdot \text{cm}^{-2}$, a factor of ten larger than the requirement for the present Tracker. Further details about the sensor R&D program can be found in [6, 7, 8].

Extensive prototyping activity is ongoing and the p_t -module working principle was demonstrated in beam tests both for 2S and PS modules [9, 10].

The Phase-2 Outer Tracker baseline layout, shown in Fig. 4, consists of six barrel layers and the endcaps with 5 disks each, for a total of 15508 detector modules (8424 2S and 7084 PS), with a total active surface of 218 m^2 , 48 M strips and 217 M macro-pixels. An alternative layout, shown in Fig. 5, is now actively pursued since it allows for a reduction of modules, material and costs. It is known as ‘tilted layout’ since part of the innermost barrel layer modules are tilted facing the interaction point to obtain the same angular coverage with a reduction of the actual sensitive surface, for a total of 13892 detector modules (8424 2S and 5468 PS), with a total active surface of 201 m^2 , 44 M strips and 174 M macro-pixels.

Figure 6: The electronics system block diagram for 2S modules.

3. The Electronic System

The electronics system, shown in Fig. 6, is designed to deliver L1 trigger and readout data with high efficiency up to a L1 trigger rate of 750 kHz, and to cope with $12.5 \mu\text{s}$ of latency.

The 2S module front-end (FE) consists of two hybrids [12], each with 8 CBC chips (CMS Binary Chips), that readout and interface the strips of the two silicon sensors. In the case of the PS module, the hybrids interface the strips, readout by dedicated Short Strip Array (SSA) chips, with the Macro-Pixel-Sub-Assembly block (MaPSA), which integrates the pixelated sensor with its readout chips (called Macro-Pixel Array, MPA). The data generated by the FE chips are buffered, aggregated and formatted by the Concentrator IC (CIC) that feeds data to the Service Hybrid(s), which hosts all services to/from the counting room: data transfer (4.8 Gb/s bidirectional multi-mode optical link based on the low speed, low power grade version of the GBT chip and the VTRx+ optoelectronic transceiver), low voltage powering (LV) and high voltage biasing (HV).

The FE and Service Hybrids are multilayer high density flexible kapton circuits that are tightly folded by design to ease connectivity to the top and bottom sensor. Both 130 nm and 65 nm technologies are likely to be used for the FE ASICs in order to achieve adequate performance while minimizing development and production costs.

At the backend, the Data, Trigger & Control Board (DTC) sends and receives data from multiple modules (typically 50 – 70 modules per card). This board is a custom development based on off-the-shelf commercial FPGAs and multi-channel optoelectronic transceivers. It processes three detector data streams: Timing and Control, DAQ and Trigger with a global usable bandwidth of 3.2 Gb/s in each direction (the raw bandwidth, including Forward Error Correction, is 4.8 Gb/s).

The DTC board sends the stub stream to the L1 track finding system. Only about 5 to 10% of the roughly 10,000 stubs per bunch crossing actually belong to $p_t > 2 \text{ GeV}/c$ primary tracks [3, 4].

Power will be supplied to the FE at a voltage of 10 – 12 V whilst the HV supply will be designed to reach -800 V . The granularity of the distribution is still under consideration. Individual supply lines to each detector module would best match the Tracker modularity and alleviate the need for complex fail-safe redundancy schemes.

Figure 7: A perspective view of the inner barrel in the 'tilted' option.

Figure 8: A detail of the module positioning in the TEDD.

4. Support Structure and Cooling

The mechanical concept of the Phase-2 Tracker is the same as for the current Tracker and consists of a support tube at the outermost radius.

The 2S modules that equip the TB2S (the three outermost barrel layers) are mounted onto ladders, 12 modules each, then installed in a support wheel that consists of 4 vertical disks joined by cylinders at the inner and outer radii.

The PS modules that equip the TBPS (the three innermost barrel layers) are glued directly onto flat composite structures in which the cooling pipes are embedded. These plates are joined and supported by vertical rings to form the cylindrical layers. Figure 7 shows the concept of the inner barrel mechanics for the 'tilted' layout where the tilted modules are supported by appropriately crafted rings.

In the endcaps the modules are mounted on flat disks, as shown in Fig. 8. These are split in half-disks, or "dees". Two disks are grouped to form one Double-Disk; ten Double-Disk units will be produced, five for each end-cap or TEDD.

The Tracker will be operated and maintained at -20°C or lower using two-phase CO_2 cooling. The total power dissipated by the Outer Tracker within the tracking volume is estimated to be around $\sim 90 \text{ kW}$. Overall the material budget of the upgraded Tracker is significantly reduced with respect to the current Tracker with a $\sim 30\%$ reduction (from $\sim 0.35X_0$ to $\sim 0.25X_0$) at $\eta \approx 0$ and a $\sim 50\%$ reduction (from $\sim 1.6X_0$ to $\sim 0.8X_0$) at larger $|\eta|$ values.

Figure 9: Track reconstruction efficiency as a function of η for $p_T = 10$ GeV/c muons (left) and $t\bar{t}$ events with $p_T > 0.9$ GeV/c and $d_0 < 3.5$ cm (centre); on the right, for $t\bar{t}$ events, the fraction of ghost tracks as a function of η . A comparison is shown between the Phase-1 detector without aging at a PU of 50 events and the Phase-2 detector at a PU of 140 events.

5. Performance

For a complete review of the L1 tracking performance of the upgraded Tracker refer to [3, 4].

Some highlights of the expected offline tracking performance [3] are shown in Fig. 9. The track reconstruction efficiency for the Phase-2 detector at a PU of 140 events for muons and $t\bar{t}$ events is as good as the Phase-1 efficiency at a PU of 50 events and extends the $|\eta|$ range by about 1.5 units thanks to the foreseen extension of the pixel detector [3, 11]. The fraction of ghost reconstructed tracks is higher but still adequate for the CMS event reconstruction.

6. Conclusions

The Phase-2 Tracker upgrade for HL-LHC consists of a replacement of the whole Tracker detector. The development of the new Outer Tracker is well advanced. The innovative module design features on-board data reduction to comply with the required L1 track trigger capabilities. The detector layout is being optimized and finalized and several R&D activities are ongoing on sensors, electronics and mechanics. The project feasibility will be demonstrated in a Technical Design Report to be published in 2017.

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