Upgrade of the ATLAS Tile hadronic calorimeter for high-luminosity LHC run

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Abstract

The ATLAS Tile Calorimeter (TileCal) will undergo a major replacement of its on- and off-detector electronics for the Long Shutdown 3 that is planned for 2024 and 2025. All signals will be digitized and transferred directly to the off-detector electronics, where the signals are reconstructed, stored, and sent to the first level of trigger at a rate of 40 MHz. This will provide better precision of the calorimeter signals used by the trigger system and will allow the development of more complex trigger algorithms. Changes to the electronics will also contribute to the reliability and redundancy of the system. Three different front-end options are presently being investigated for the upgrade and will be chosen after extensive test beam studies. A Hybrid Demonstrator module has been developed. The demonstrator is undergoing extensive testing and is planned for insertion in ATLAS.

Keywords: ATLAS; LHC; Tile calorimeter; Upgrade; FPGA.

1. The Tile Calorimeter

The TileCal is the central hadronic calorimeter within the ATLAS detector (Figure 1) at the Large Hadron Collider (LHC) situated at CERN, Geneva [1]. The calorimeters have the essential role of providing precise measurements (energy and angle) of hadrons, jets, taus and missing transverse energy during proton-proton collisions. The TileCal is composed of four barrel sections (two central and two extended barrels), each containing 64 azimuthal slices. Each slice consists of alternating steel plates and plastic scintillating tiles. Wave-Length Shifting (WLS) fibres are coupled to each tile cell to collect the produced light and are readout by photomultiplier tubes (PMT) located inside mechanical supports called drawers. There are more than 5000 tile cells, each being readout by two PMTs. Drawers are found within the outer section of each TileCal slice, drawers also contain the on-detector electronics. An analog sum of the processed signal of several PMTs serves as input to the level 1 (L1) trigger. Signals from the PMTs are shaped, amplified and digitised with a 10 bit ADC at 40 MHz and are stored in temporary pipeline memories on-detector while they wait for the L1 acceptance trigger.

2. Upgrade Motivation and requirements

The upgraded High Luminosity LHC (HL-LHC) is planned to be ready by 2026, leading to an increase in design luminosity by a factor of 5 to 10 [2]. This presents many design challenges as electronics will need to withstand a much higher radiation dose as well as a increased demand for data throughput. The current ATLAS electronics are coming to the end of their design lifespan and with the new HL-LHC design requirements there is a need for a complete replacement and redesign of both the on- and off-detector electronics of the ATLAS TileCal [3]. The ATLAS detector was completed in 2008 and since then there

Figure 1: Cross-sectional view of the central ATLAS detector.

have been significant advances in FPGAs, ASICs, component radiation hardness and data throughput for which the upgrade plans to take advantage. New levels of redundancy and modularity will be introduced into the on-detector electronics and power supplies, increasing reliability and allowing for easier extraction and repair during shutdowns [4]. A Hybrid demonstrator has been developed to test the newly proposed architecture while also providing compatibility with current legacy systems.

3. Current electronics

The present on-detector electronics architecture is based on a four board design: 3-in-1 Front-end Board (FEB), Digitizer board, interface board and Trigger sum board. The data flow can be seen in Figure 2. The current 3-in-1 FEB amplifies (Bi-gain $\times 1$, $\times 64$), shapes PMT signals and provides calibration functions. Analog signals are sent from each FEB to the adder board which forwards the tower sums over 90 meters to a

off-detector trigger processor. Signals from the FEBs are digitised at bunch crossing frequency and data is stored locally in pipeline memories pending a L1 Trigger accept. If data is validated by L1 it will be sent to the local interface board and placed in derandomising buffers before being sent off-detector to the Read-Out Driver (ROD) to be formatted and sent to the Data Acquisition system (DAQ). The L1 trigger selection is able to reduce the data rate coming from the PMTs at a bunch crossing frequency of 40 MHz to a rate of 100 kHz to the ROD.

Figure 2: TileCal signal flow in the current system.

4. Electronics Upgrade

The new upgrade architecture fully digitises all detector signals and sends them off-detector through high throughput optical links to the Preprocessor (TilePPr) [5]. This approach allows the maximum amount of information to be made available for the trigger, improving precision and granularity. The data flow for the upgraded architecture is shown in Figure 3. The on-detector electronics is housed within long insertable modules called superdrawers. Each superdrawer can be mechanical divided into 4 separate minidrawers to aid with extraction and repair. A minidrawer can host up to 12 PMTs, 12 FEBs, a Main-board (MB), a Daughterboard (DB), a high voltage board and Analog Adder board (Hybrid only).

Figure 3: TileCal signal flow for HL-LHC upgrade.

Three alternative FEB strategies have been proposed and are currently undergoing feasibility studies. Two FEB options are based on custom ASIC designs (QIE and FATALIC), the other is an updated version of the current 3-in-1 FEB which is currently used for the Hybrid Demonstrator. Each FEB option allows for the calibration of electronics, PMT gain and scintillator response. The 3-in-1 FEB strategy consists of a LC shaper, two clamping amplifiers (low and high) for fast signal processing and a slow integrator (Figure 4). The slow integrator is used to monitor the minimum bias current of the PMTs during collisions and the Charge Injection and Cesium calibrations (CIS). The two amplified fast signals are sent via a differential cable to the MB for digitisation by a 12-bit 40 Msp/s ADC, covering a dynamic range of 17 bits.

Figure 4: Diagram of the analog front-end readout electronics.

The two other FEB strategies are still in development. The Charge Integrator and Encoder (QIE) [6] (Figure 5), has no pulse shaping and has self signal digitisation at four gain ranges see ref. [7]. The "all in one" FEB is based on the TileCal integrator circuit (FATALIC) ASIC (Figure 6) which make use of a current conveyor [8] and radiation hard ADCs which use three 12-bit gain ranges.

Figure 5: QIE signal flow

Figure 6: FATALIC basic circuit architecture.

The MB interfaces with 12 PMTs, providing signal digitisation, synchronised sampling clocks and data forwarding to the DB. The new 3-in-1 compatible MB [9] has improved on the current design and uses discrete commercial-off-the-shelf (COTS) components.

The DB gathers digitised signals from each FEB before sending them through two multi-gigabit optical cables to the TilePPr. All communications with on-detector electronics are controlled by the DB. Data is uploaded from the DB at a rate of 9.6 Gbps and data streams received from the TilePPr are encoded in the GBT protocol at 4.8 Gbps for drawer configuration and timing. To improve reliability each half of the DB is managed by a Kintex-7 FPGA, with additional redundancies on the FPGAs themselves.

Once data signals reach the TilePPr they undergo reconstruction and are distributed to the trigger. As the pipeline memories have now been moved off-detector to the TilePPr, more efficient, non-radiation hard components can be used. The TilePPr is responsible for sending trigger tower signals, receiving/sending slow controls to the drawers and establishing system timings for the synchronisation of readout and the DAQ. The TilePPr incorporates both a Xilinx Virtex-7 and Kintex-7 FPGA with 4 Quad Small Form Factor Pluggable (QSFP) optical transceivers (Figure 7).

Figure 7: First prototype of the TilePPr.

The upgraded power distribution system has three stages (Figure 8). The Low Voltage Power System (LVPS) is located at the outer end of each tile module. The LVPS (stage 2) receives bulk 200V and produces two independent +10V lines per minidrawer using switching power generation techniques [10]. The LVPS system is divided into 8 independent +10V power "bricks" that serve 4 minidrawers. Two +10V lines are received by each mainboard and are distributed to the many subsystems within the minidrawer. These +10V supplies are regulated using Point Of Load (POL) regulators to produce 9 different voltages needed by the front-end circuits. The minidrawer system is designed such that each subcomponent has a split power distribution system, with each half being powered by a separate +10V brick. This redundancy was implemented in case of a LVPS brick failure, the second brick can thus provide power to both halves

Figure 8: Block diagram of the power distribution system for a Super Drawer.

5. Upgrade status and performance

5.1. TilePPr

The first TilePPr prototypes have been designed, produced and evaluated as part of the TileCal demonstrator project. To evaluate the signal integrity of the QSFP lines, a Xilinx IBERT IP core was implemented in firmware using an external optical lookback. Bit-Error Ratio (BER) tests were performed using a PRBS-31 data pattern running at 9.6 Gbps on sixteen links. No errors were observed during a data taking period of 115 hours, corresponding to a $\text{BER} \leq 5 \cdot 10^{-17}$ with a confidence of level of 95% [11]. The eye diagram in Figure 9 was obtained using the IBERT IP core on the GTX transceivers used for both uplink and downlink communication paths.

Figure 9: a) Eye diagram at 4.8 Gbps and b) Eye diagram at 9.6 Gbps. [11]

Firmware was originally developed using a Xilinx VC707 evaluation board but has been successfully migrated to TilePPr. The system has the ability to operate and read-out the TileCal demonstrator module using asymmetric GBT links (4.8 Gbps / 10.24 Gbps) with clock synchronisation between transmission and reception being performed by internal dual FIFO memories. Remote operation of the TilePPr is managed using a set of C++ and Python scripts through GbE ports using the IPBus for monitoring, data taking and calibration. The TilePPr was successfully used for the evaluation of the demonstrator during the October 2015 test-beam operations and will be used again during the next test beam in June 2016.

5.2. Hybrid demonstrator

A complete functional Hybrid Demonstrator has been built and is currently undergoing testing. All on-detector systems are undergoing radiation testing to simulate the detector environment during the HL-LHC. Four possible radiation cases were looked at: expected Total Ionising Dose (TID) during HL-LHC, Single Event Upsets (SEE) of a high radiation environment, particle displacement damage effects and Non-Ionising Energy Loss (NIEL). Automatic data scrubbing has been implemented with Triple Mode Redundancies (TIR) within the FPGAs to counter SEE events on the DB.

General demonstrator performance has been measured through the three calibration systems. The CIS directly tests the electronics by injecting a known charge into the FEB to mimic a PMT signal. Results show good control and linearity in the high and low gain fast readout channels (Figure 10). The Laser calibration system is able to test the PMTs by flashing light

pulses of a known intensity into a PMT. This allows for the calibration of the PMT gain levels and trigger timings to be set. The Cesium calibration system moves a radioactive Cesium-137 source through a TileCal slice to measure the response of the whole system (Scintillator/PMT/electronics). Cesium scans were performed on the demonstrator system (Figure 11). After extensive testing the demonstrator is behaving as expected and is nearly ready for insertion into the ATLAS detector.

Figure 10: Integrator response over time to a Cesium Source in Extended Barrel Cell D-6. <https://twiki.cern.ch/twiki/bin/view/AtlasPublic/ApprovedPlotsTile>

Figure 11: Characteristic sharp peaks as the source passes each of the 75 individual scintillator tiles. <https://twiki.cern.ch/twiki/bin/view/AtlasPublic/ApprovedPlotsTile>

6. Conclusion

The Tile Calorimeter Phase II upgrade is far into its development and a demonstrator module has been produced. Component and design revisions are ongoing in order to improve performance. Control and calibrations tests have proved successful in the demonstrator, all legacy systems have been interfaced. The test beam was during two weeks in October 2015. We will have two more test beam campaigns in summer and fall 2016.

References

[1] ATLAS Collaboration 2008 *Journal of Instrumentation* **3** S08003 URL <http://stacks.iop.org/1748-0221/3/i=08/a=S08003>

[2] ATLAS Collaboration 2015 ATLAS Phase-II Upgrade Scoping Document Tech. Rep. CERN-LHCC-2015-020. LHCC-G-166 CERN Geneva URL <https://cds.cern.ch/record/2055248>

[3] Tang F, Anderson K, Akerstedt H, Bohm C, Carrio F, Drake G, Hildebrand K, Muschter S, Oreglia M, Paramonov A and Valero A 2013 Upgrade analog readout and digitizing system for atlas tilecal demonstrator *Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC)*, 2013 *IEEE* pp 1–6

[4] ATLAS Collaboration 2012 A hybrid readout system for the ATLAS TileCal phase 2 upgrade demonstrator *Proceedings, 2012 IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC 2012): Anaheim, California, USA, October 29-November 3, 2012* pp 1416–1419 URL <http://inspirehep.net/record/132465>

[5] ATLAS Collaboration 2015 A new read-out architecture for the ATLAS Tile Calorimeter Phase-II Upgrade Tech. Rep. ATL-TILECAL-PROC-2015-025 CERN Geneva URL <https://cds.cern.ch/record/2117093>

[6] Hoff J 1999 SMQIE: The Shower Max QIE chip Tech. Rep. FERMILAB-TM-2075 Fermi National Accelerator Laboratory Batavia URL <http://inspirehep.net/record/501280>

[7] Drake G, Paramonov A, Proudfoot J, Stanek R and Chekanov S 2015 QIE12: A New High-Performance ASIC for the ATLAS Tile-Cal Upgrade *Topical Workshop on Electronics for Particle Physics* URL <https://cds.cern.ch/record/2058155>

[8] ATLAS Collaboration 2013 *EPJ Web Conf.* **60** 20057. 3 p URL <https://cds.cern.ch/record/1558365>

[9] Tang F, Akerstedt H, Anderson K, Bohm C, Hildebrand K, Muschter S and Oreglia M 2013 Upgrade Analog Readout and Digitizing System for ATLAS TileCal Demonstrator *IEEE Transactions on Nuclear Science* ISBN 9781479905348 ISSN 00189499

[10] Drake G 2013 *Journal of Instrumentation* **8** C02032 URL <http://stacks.iop.org/1748-0221/8/i=02/a=C02032>

[11] Carrio Argos F and Valero A 2015 Performance of the Tile Pre-Processor Demonstrator for the ATLAS Tile Calorimeter Phase II Upgrade Tech. Rep. ATL-TILECAL-PROC-2015-018 CERN Geneva URL <http://cds.cern.ch/record/2067612>