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Status of sensor qualification for the PS module with on-chip p_T discrimination for the CMS tracker phase 2 upgrade

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The high luminosity upgrade of the LHC is targeted to deliver 3000 fb^{-1} at a luminosity of $5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. Higher granularity, 140 collisions per bunch crossing and existing bandwidth limitations require a reduction of the amount of data at module level. New modules have binary readout, on-chip p_T discrimination and capabilities to provide track finding data at 40 MHz to the L1-trigger. The CMS collaboration has undertaken R&D effort to develop new planar sensors for the pixel-strip (PS) module, which has to withstand $1 \times 10^{15} \text{ cm}^{-2}$ 1 MeV neutron equivalent fluence in the innermost layer of the tracker. The module is composed of a strip sensor and a macro pixel sensor with $100 \mu\text{m} \times 1.5 \text{ mm}$ pixel size. Sensors were characterized in the laboratory and the effects of different process parameters and sensor concepts were studied. This contribution presents a new sensor prototype with n-pixels in p-bulk material in planar technology for the PS module. A new inverted module concept is presented, which has advantages with respect to the baseline concept. Electrical characterization of sensors and SEM-images are presented.

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Status of sensor qualification for the PS module with on-chip p_T discrimination for the CMS tracker phase 2 upgrade

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Abstract

The high luminosity upgrade of the LHC is targeted to deliver 3000 fb^{-1} at a luminosity of $5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. Higher granularity, 140 collisions per bunch crossing and existing bandwidth limitations require a reduction of the amount of data at module level. New modules have binary readout, on-chip p_T discrimination and capabilities to provide track finding data at 40 MHz to the L1-trigger. The CMS collaboration has undertaken R&D effort to develop new planar sensors for the pixel-strip (PS) module, which has to withstand $1 \times 10^{15} \text{ cm}^{-2}$ 1 MeV neutron equivalent fluence in the innermost layer of the tracker. The module is composed of a strip sensor and a macro pixel sensor with $100 \mu\text{m} \times 1.5 \text{ mm}$ pixel size. Sensors were characterized in the laboratory and the effects of different process parameters and sensor concepts were studied. This contribution presents a new sensor prototype with n-pixels in p-bulk material in planar technology for the PS module. A new inverted module concept is presented, which has advantages with respect to the baseline concept. Electrical characterization of sensors and SEM-images are presented.

Keywords: CMS tracker upgrade, silicon sensors, module with on-chip logic, particle detector

1. Introduction

The current CMS tracker [1] needs a major upgrade, which is developed for an integrated design luminosity of 3000 fb^{-1} at an instantaneous luminosity of $5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ during the HL-LHC phase [2]. In the legacy tracker system the L1-accept rate is limited to 100 kHz. It will be increased up to 750 kHz in the high luminosity period. For the current sensor technology with p-strips in n-bulk material the increasing full depletion voltage and increasing leakage current of the sensors lead to a situation where the bias voltage and necessary cooling power get close to the limits of the current system. Sensors cannot be depleted, which implies a complete loss of the signal. During HL-LHC the CMS tracker must work at an estimated pile-up of 140 at 25 ns bunch spacing. This has to be addressed at module level. Binary readout of the modules and on chip p_T -discrimination is therefore necessary, in order to include the tracker in the trigger decision and to reduce the data rate.

2. PS module for the CMS phase 2 Upgrade

For the upgrade of the tracker two different types of modules are foreseen: The 2S module which contains two silicon strip sensors with $100 \mu\text{m}$ pitch, and the PS-module [2, 3]. The PS-module consists of a pixel and a strip sensor of n in p-bulk technology (Fig. 1, 2). For testing purposes a smaller prototype sensor was designed and processed. This so-called PS-p light

sensor has 6 rows of 38 columns of $100 \mu\text{m} \times 1.6 \text{ mm}$ pixels and a width to pitch ratio of 0.25. The foreseen readout chip is the Macro Pixel ASIC (MPA) with integrated stub finding logic for p_T -discrimination [4]. A MPA-light demonstrator chip reads out 3 rows of 16 pixels. A total of 6 MPA-light chips are bump-bonded to a PS-p sensor (Fig. 3). The sensors implant width is $125 \mu\text{m}$ and the pitch is $200 \mu\text{m}$ at the readout chip boundaries. The n-pixels are directly connected to the chip and a punch-through-protection (PT) structure is implemented to test sensors before bump bonding and ensure the homogeneity of the electrical field in case of accidentally not connected bonds, as well as to protect the chip in case of beam loss scenarios. The PT-structure behaves analog to a transistor in weak inversion and the current from source to drain is dominated by diffusion at the working point. Surface resistivity and p-stop concentration, p-stop width and geometry adjust the current. $200 \mu\text{m}$ thickness of the active volume was selected and n-in-p technology was chosen as a result of previous studies [5].

Figure 1: Exploded view of the PS-module and cross section through the module from technical proposal [2].

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Figure 2: Standard PS-p sensor layout with indication for the edge ring geometry.

Figure 3: Bump-bonded PS-p light sensor with 6 MPA-light chips.

Variant	Doping conc. [cm ⁻³]	Implant depth [μm]	Strip isolation	V_{dep} [V]
1	1×10^{16}	1.5	p-stop	41.7 ± 1.5
2	1×10^{16}	2.5	p-stop	75.5 ± 3.8
3	1×10^{17}	2.5	p-stop	80.6 ± 1.8
4	2×10^{15}	0.5	p-spray	41.8 ± 3.6

Table 1: Prototype variants with the specified process parameters produced and measured median and standard deviation of V_{dep} .

3. Prototype sensors and testgroups

Sensors were produced in 4 different flavours (Table 1). Strip isolation was realized with p-stop implants in atoll configuration and for one of the produced variants the p-spray technique was applied. The aim was to study the effects of different p-stop concentrations and depths, and p-spray on sensor parameters, such as single strip current (I_{strip}), interstrip Resistance (R_{int}), punch-through resistance (R_{PT}) and noise. Sensors with three different edge ring widths were produced (Fig. 2). Smaller edge ring width improves the geometric efficiency, but may deteriorate the high voltage stability, increase the dissipated power in the cooling system and increase the probability for microdischarge.

4. PS module inverted concept

The PS module inverted concept flips sensor and readout chip in the module (Fig. 4). The advantages are no scattering material between the two sensors, which may have positive effects on the on-chip discrimination logic and better cooling of the chip. The concept avoids to have bump-bonding and wire-bonding on the readout chip, which is not provided by the foundries in the process. For this inverted configuration a sensor with a special routing area for low voltage and digital I/O connections for the readout chip was produced (Fig. 5). A drawback may be increased noise due to bulk coupling of signals on the sensor.

Figure 4: Inverted PS module with sensor and chip flipped.

Figure 5: The sensor layout with routing area for the inverted concept.

5. Electrical characterization of sensors

Measurements on the global parameters of the sensors were conducted using a Keithley K237 source measure unit and a high precision LCR-meter. The number of samples per test-group (Table 1) is 5 for the standard design, 2 for the inverted geometry, and 4 for the edge ring geometries.

Figure 6: The IV-curves of standard design show early breakdown for variant 3.

Figure 7: Representative IV-curves, for variant 2 for different edge geometries show small impact on the breakdown voltage and slightly higher currents for smaller edge width.

From the IV-characteristic of the baseline sensor design in Fig. 6 one concludes that the HV-stability of the variant 3 is reduced, due to the high electric fields caused by the high p-stop concentration. This is expected from simulations [6]. The sensor currents are lower for a p-stop depth of 2.5 μm, which results mainly from the different resistance of the PT-structure.

Figure 8: The inverted geometry IV-characteristic is compatible with the standard design and small additional currents are picked up in the routing area for the p-spray variant.

A smaller edge ring width is desirable to increase the active area of the sensor. The impact of (350, 500 and 850) μm width of the edge ring (Fig. 7) on the breakdown voltage is not visible and for smaller edge ring widths the currents are slightly higher. Fig. 7 shows a representative selection of IV-curves for variant 2. The currents for the inverted geometry (Fig. 8) are slightly higher compared to the standard layout. The p-spray sample has a higher current, which possibly originates from the routing area.

Figure 9: CV-characteristic for the standard geometry shows two groups for V_{dep} , which to some extent may be caused by differences in flatband voltage.

The capacitance-voltage (CV) characteristic of the sensors (Fig. 9, 10) shows different depletion voltages for both standard and edge ring designs (Table 1), which is currently under investigation. The end capacitance and depletion voltage are grouped for variant 2 and 3, which have the same p-stop implant depth. The end capacitance and depletion voltage for the edge ring geometries is compatible with the standard geometry. The difference in the depletion voltage has been confirmed by CV measurements on diodes. From the CV-characteristic of MOS-structures one deduces a flatband voltage of (3 ± 1) V for Variant 1 and 2. For variant 3 the flatband voltage at 500 Hz is 20 V and frequency dependent. The difference in flatband volt-

Figure 10: Samples with different edge width from all variants have the same end capacitance as the standard design.

Figure 11: The CV-characteristic of the inverted geometry is compatible with the standard geometry.

age may have a small impact on the depletion voltage, but additional effects are necessary to explain the difference. P-spray and a low p-stop implant depth lead to higher end capacitance. The samples for inverted geometry (Fig. 11) have a small negligible additional capacitance, which may originate in the routing area, and the end capacitance is compatible with variant 1 and 4 in standard design. Higher end capacitance for the p-spray type may arise due to insufficient isolation of the routing area.

5.1. Stripsan results

The pixel currents were measured within an automated strip-scan and optical inspection was done to investigate the defective pixels with high currents (Fig. 12). These pixels could be traced back to scratches found during the optical inspection. The pixels are mapped to 6 lines of 48 columns. For line 0 and line 5 (Fig. 13) slightly higher currents due to edge effects were observed. The number of defective strips is at the 1 % level and smaller for sensors without visible mechanical damage. For variant 1 the sum current of all pixels exceeds the global dark current and I_{strip} is low at the edges of lines 1 to 4 and increases towards the midpoint of a line. This indicates that current from neighbouring strips is picked up and pixel separation along the lines is insufficient. This is in accordance with R_{int} measurements. The

p-spray variant shows reduced interstrip isolation in the order of $R_{\text{int}} = 1 \text{ k}\Omega$, which is due to the fact that the mask for the PT-structure was the same as for p-stop isolation and p-spray dose too low for the PT-structure, but appropriate for strip isolation and HV-stability. Pixels at the boundaries of the readout chip have higher currents, as expected. During the optical inspection it was found that the PT-structure is at the lower limit of the feature size of the used process. This may be a reason for the broad distribution of the breakdown voltages.

Figure 12: The currents measured at $V_{\text{bias}} \approx 1.7V_{\text{dep}}$ for five different sensors. Bigger pixels at the readout chip borders have increased current. Red lines separate the rows.

Figure 13: A map of the pixel currents to the sensor geometry. Three pixels with high current are visible, which could be traced back to scratches in the optical inspection.

6. SEM imaging

The layer thickness of passivation, metal and oxide is of general interest and can be used as input for simulations. For this purpose samples were cut, ground and polished with diamond polish of 10 nm grain size. Buffered HF and HNO_3/HF solution was used to etch the sensor and generate a topological contrast and a contrast for the doped area. Scanning electron microscopy (SEM) images were taken at a cut through the metal

Figure 14: SEM image at 10 kV ac- Figure 15: A cut through the PT-structure. A cut through the structure. a strip.

Layer	Thickness [nm]
Strip passivation	515
Strip aluminum	1440
Strip dielectric	132
Backplane aluminum	1520

Table 2: Layer thickness obtained from SEM imaging.

strip contacts, the PT-structures and through the strips (Fig. 14,15).

The layer thickness (Table 2) was measured at magnification of 50×10^3 and acceleration voltage of 10 kV, which ensures good contrast for the secondary electron analysis for low Z-material. For the inner aluminum circles of the PT-structure small deformations were seen and non concentric circles in the PT-structure were observed, which may have an impact on the HV-stability.

7. Conclusion

Sensor prototypes for the PS module of the tracker upgrade were produced and characterized. Sensor qualification is ongoing and prototype modules are built. Different process parameters were studied. The sensor design was verified and studies on the inverted geometry show promising results. A low number of defective pixels was observed. Studies on the quality of bump bonding and tests with particles are ongoing and show good results.

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