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1-Grad total dose evaluation of 65 nm CMOS technology for the HL-LHC upgrades

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Abstract: The radiation tolerance of 65 nm bulk CMOS devices was investigated using 10 keV X-rays up to a Total Ionizing Dose (TID) of 1 Grad. Irradiation tests were performed at room temperature (25°C) as well as at low temperature (−15°C). The implications on the DC performance of n and p channel transistors are presented. For small size devices, a strong performance degradation is observed from a dose of 100 Mrad. Irradiations made at room temperature up to 1 Grad show a complete drive loss in PMOS devices, due to decreasing transconductance. When the irradiation is conducted at −15°C, the devices show less radiation damage. Annealing helps recovering a small part of the drive capabilities of the small size devices, but the threshold voltage shift is still high and might compromise the operation in some digital applications.

Keywords: VLSI circuits; Radiation-hard electronics

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1 Introduction

The High Luminosity LHC (HL-LHC) is the proposed upgrade to the LHC to be made in a long machine shutdown which should take place in the years 2023 to 2025, according to current schedule. The upgrade aims at increasing the luminosity of the machine up to $5 \times 10^{34} \text{ cm}^{-2} \text{s}^{-1}$. The upgrade will improve statistically marginal measurements and will allow a better chance to see rare processes.

The ATLAS and CMS experiments are planning major detector upgrades to cope with the increase in beam luminosity. Pixel detectors are placed in the innermost part of the experiments and are therefore exposed to the highest fluences and highest ionizing radiation doses. Simulations show that the innermost parts of the new pixel detector will integrate a fluence of about $10^{16} \text{n/cm}^2$ (1 MeV neutron equivalent) and a Total Ionizing Dose (TID) of 1 Grad.

The RD-53 collaboration [1] was established to develop the next generation of pixel readout chips needed by ATLAS and CMS at the HL-LHC. This development requires extreme rate and radiation tolerance. The 65 nm CMOS process seems to be promising for the future pixel readout...
chips in terms of high integration density, but has to be extensively tested and qualified for the radiation environment. A lot of information can be obtained by studying radiation effects on individual transistors, as a way to understand the causes of failure in digital or analog designs.

This work investigates, for the first time, the TID effects in 65 nm NMOS and PMOS core transistors up to 1 Grad. It has been made within the framework of the RD53 collaboration.

In section 2, we analyse briefly the effect of irradiation on the highly scaled CMOS technology. In section 3, we describe the test set up and the facility used for device irradiation and testing. In section 4, we present the most important results related to the dose effect on the TSMC 65 nm process (CERN frame contract) at room temperature. Experimental results from irradiation at low temperature are presented in section 5, where the results from studies on another 65 nm process are also given for comparison. In section 6, we provide a short analysis and discussion concerning the effects observed.

2 Radiation effects in “modern” CMOS processes

Figure 1 shows the cross section of an NMOS device in a highly scaled CMOS process. From the point of view of radiation effects, the most sensitive parts of a MOSFET are the oxide insulators.

The gate oxides of advanced CMOS technologies are scaled to thinner dimensions, which should reduce the shifts in DC parameters due to the trapped charge buildup in the gate oxide. Furthermore, the tunnel effect removes the trapped charge near the interface. This reduces the shifts in DC parameters resulting from interface charges. Therefore, it can be concluded that a modern commercial process such as the 65 nm process considered in this study should be intrinsically radiation hard for what concerns gate-oxide related DC parameter shifts.

A Shallow Trench Isolation (STI) is used in this process as the field oxide for device isolation and is thought to be the main issue when considering TID effects for scaled down technologies as indicated in recent studies [2]. STI effects are there thought to be related to radiation-induced oxide traps and interface trap build-up along or near the STI sidewall. Positive oxide charge trapped in the lateral STI oxide, particularly at the Si/SiO interface along the edge of the transistor, induces a leakage path. This parasitic STI device contributes to the increase of the leakage current in the irradiated NMOS devices. The degree to which the channel close to the STI can invert is also
inversely proportional to the doping concentration along the sidewall [3]. Actually, a higher doping concentration will typically mitigate the effects of fixed oxide trapped charge in the STI.

In some processes, a silicon nitride spacer is added to reduce parasitic resistance. It allows implantation of a deeper level of drain or source diffusion. The degradation of device characteristics can then be attributed to the positive charge induced in the spacer’s oxide because of irradiation effects.

3 Devices and experimental set up

The devices used in this study are n and p channel MOSFETs manufactured using the TSMC commercial 65 nm low-power technology developed for logic and mixed-signal applications. Only the core transistors are considered in this study. The nominal supply voltage is 1.2 V and an STI field oxide with a thickness of about 400 nm is used to isolate one device from the other. This process allows the implementation of devices with different threshold voltages in the same chip, depending on the application requirement.

3.1 X-ray Test Set-up

In order to study the irradiation tolerance of the devices for the environment of the HL-LHC pixel detector, the level of dose has to be brought as high as 1000 Mrad (SiO2). Irradiation tests were performed using CERN’s 50 kV 3 kW X-ray generator (SEIFERT RP149) as shown in figure 2. A Keithley 2636A Source Measurement Unit (SMU) associated to a Keithley 707 switching matrix was used to build a complete automated test set up for performing the static transistor measurements. All the instruments were controlled by a PC running Labview software, allowing high speed measurements with very high precision in voltage and current. The set-up is able to test up to 20 devices sequentially and can be easily upgraded to test 80 different devices.

Figure 2. CERN X-ray Test Set-up: (a) (b) test set up comprising a Keithley 2636A SMU and a Keithley 707 switching matrix (c) wire-bonded chip placed under the Xray source.
Table 1. Tested devices.

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<td>FOXFET devices</td>
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This irradiation study was performed at two different temperatures, room temperature (25°C) and −15°C, at a dose rate of about 9 Mrad/hour (2.5 kRad/s). The chip was irradiated in steps up to a maximum TID of 1000 Mrad and devices were kept at a bias expected to allow the highest degradation during irradiation and annealing. For the NMOS devices, the bulk and source terminals were grounded while the gate and the drain terminals were set to 1.2 V. For the PMOS devices, the bulk and the source terminals were kept to 1.2 V while the gate and the drain terminals were set to 0 V.

3.2 Tested devices

The test chip was designed by the CERN microelectronics group [4]. It contains single transistors arranged in arrays of given channel width or length with common gate, source and bulk terminals and separated drain contacts. Arrays were provided with a protection diode at the common gate.

Since the dominant TID effect was thought to be the charge build-up in the STI, the parasitic transistors could be considered as the main source of degradation. This is the reason why devices with different widths were considered in this study, all with minimum length of 60 nm. Only the Standard Threshold Voltage (SVT) devices were studied here. Note also that an enclosed layout geometry transistor was tested for comparison. Testing the radiation tolerance of the devices of different sizes shown in table 1 will help in setting the minimum width for PMOS and NMOS transistors to be used in digital design libraries for the HL-LHC high radiation environment.

Electrical measurements were made before irradiation, then after doses of 100 kRad, 1 Mrad, 10 Mrad, 100 Mrad and then at steps of 100 Mrad up to a maximum of 1000 Mrad (where doses are expressed in SiO2).

TID testing and qualification was typically performed at a High Dose Rate (HDR) of 9 Mrad/hour; several orders of magnitude higher than the Low Dose Rate (LDR) anticipated in the future HL-LHC environment. The qualification for LDR environments consists in performing HDR testing followed by an annealing operation under bias. The annealing schedule consisted of three stages, first with the devices biased and tested at low temperature, then at room temperature for a few days, and finally for one week at high temperature (100°C). Regular measurements were performed throughout these phases.
4 Results at room temperature

4.1 Irradiation effects on NMOS devices

4.1.1 Leakage current variation

The off-state leakage current is defined as the drain-source current for $V_{GS} = 0$ V. The increase of off-state leakage current with radiation represents one of the main issues in advanced deep submicron bulk CMOS transistors.

Figure 3a shows the variation of the leakage current versus the TID for devices of different sizes. For a dose level of 1 Grad, the leakage current of the narrower device (120 nm/60 nm) increases by a factor 100, whereas this increase is limited to 2 to 4 times the pre-irradiation value for enclosed and wider devices.

It may be recalled that the 130 nm process used for the ATLAS pixel detector FE-I4 design showed a higher leakage current. The minimum size NMOS device (160 nm/120 nm) exhibited a leakage current of about 100 nA after 100 Mrad [5], a three orders of magnitude increase with respect to pre-irradiation value.

Figure 3b shows the leakage current variation for different FOXFET devices as a function of the TID level. This results indicates that the inter device leakage increase is less than 20 times the pre-irradiation value and the absolute value is less than 100 pA even up to a dose level 1 Grad.

From the point of view of the leakage current, we can conclude that the TSMC 65 nm devices exhibit better performance compared to the 130 nm technology used in the present generation of pixel readout chip designs. With respect to the issue of leakage current after irradiation, these results suggest the possibility of using NMOS core transistors without special layout protection.

4.1.2 DC drain current degradation

Figure 4a shows the $I_{DS}(V_{GS})$ curves obtained on a minimum size NMOS transistor (120 nm/60 nm). The curves are plotted for different levels of radiation and they clearly show that the drain current increases slightly for low dose levels before turning over and decreasing strongly at higher dose levels.
Figure 4. NMOS characteristics variation as function of TID for 120 nm/60 nm NMOS biased at $V_{DS} = 50 \text{ mV}$ ($T = 25^\circ \text{C}$) (a) $I_{DS}(V_{GS})$ characteristics and (b) transconductance.

Figure 5. NMOS DC parameters as a function of the TID level at $25^\circ \text{C}$ (a) Current drive variation (for $V_{DS} = 1.2 \text{ V}$) (b) Threshold voltage shift (extracted for $V_{DS} = 50 \text{ mV}$).

Figure 4b represents the NMOS device transconductance as function of the gate voltage for different TID levels. For high TID, the transconductance peak value significantly decreases and shifts to higher values of $V_{GS}$. The current driving loss can thus be attributed to both the threshold voltage shift and to the mobility decrease (transconductance factor).

For a given drain voltage $V_{DS}$, the maximum current flowing through a device occurs at the maximum gate voltage ($V_{GS} = 1.2 \text{ V}$). The variation of this current drive can be used to measure the degradation in a given device, as shown in figure 5a, which represents the variation of this parameter as a function of the TID level when devices are biased in the saturation region ($V_{DS} = 1.2 \text{ V}$).

Additionally, we must consider other device parameters in order to estimate the impact of such a degradation on the circuit operation. In this study, we consider the threshold voltage (VTH) for which the calculation is based on the method of extrapolation from the linear region. This consists of defining the extrapolation curve of the $I_{DS}(V_{GS})$ characteristics at its maximum first derivative (maximum transconductance) [6].

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Figure 4.

Figure 5.
Figure 6. PMOS characteristics variation versus TID at 25°C (a) $I_{DS}(V_{GS})$ for 120 nm/60 nm PMOS and (b) transconductance for 480 nm/60 nm PMOS device.

The threshold voltage as a function of the TID level is plotted in figure 5b, where we can distinguish two major regions:

- the region for TID levels below 100 Mrad where the narrowest devices show an increase of the current drive. This change is relatively small. It is limited to 7% for the narrowest device (120 nm/60 nm) and no variation is observed for wide or enclosed devices. In this region, the threshold voltage shift is negative and depends on the device width. For the minimum size device, a negative shift of 15 mV is measured at the dose level around 10 Mrad;

- the region of high dose level (beyond 100 Mrad) where a strong loss of the drive current is observed for all tested devices. For a TID of 1 Grad, the degradation of the NMOS devices drive current is between 48% and 66% with respect to pre-irradiation values. In this region, the threshold shift is positive and tends to turn off all NMOS devices. In these measurements, the threshold shift reaches a value of 350 mV for the TID level of 1 Grad and seems to have little dependence on the transistor width. Moreover, even the enclosed NMOS device shows a positive $V_{TH}$ shift of 250 mV at 1 Grad which is still quite large (albeit lower than the shift experienced for the open geometry devices). In fact, we expected a lower degradation than observed, since edgeless devices are known to be very tolerant to the dose effects.

4.2 Irradiation effects on PMOS devices

As in the NMOS device, positive charge trapping in the dielectrics should change the electrostatic potential in the PMOS transistor and consequently change its DC characteristics.

This phenomenon seems to be confirmed in figure 6a, where the $I_{DS}(V_{GS})$ curves obtained on a narrow 0.12 µm PMOS transistor are plotted for different levels of TID. This shows clearly that the device becomes completely turned off at TID levels exceeding 600 Mrad.

Figure 6b shows the variation of the transconductance as a function of the gate voltage for the 480 nm/60 nm PMOS device. It can be seen that the transconductance peak decreases when the level of the total dose increases — as in the case of the NMOS devices — but for the PMOS device
the peak does not shift. This suggests that the current drive loss can be mostly attributed to mobility degradation (transconductance factor) rather than to the threshold voltage shift.

Figure 7a shows the variation of the current drive as function of the TID level. A large reduction in the current drive is observed for the PMOS devices, and reaches 100% at the highest dose in the case of the narrow devices (120 nm/60 nm and 240 nm/60 nm). PMOS devices show more degradation than the NMOS devices, and this degradation is clearly correlated to the device width. For the transistor of width 480 nm, the degradation at 1000 Mrad is around 80%; it is 70% for the 1 µm one, but is limited to 40% for the enclosed device.

Figure 7b shows the shift of the threshold voltage versus the TID. The $V_{TH}$ shift of the narrowest devices is not plotted because the devices become practically turned off, preventing the $V_{TH}$ extraction from the $I_{DS}(V_{GS})$ characteristic. The threshold voltage shift has been extracted on open geometry PMOS transistors of sizes 480 nm/60 nm and 1000/60 nm, and an enclosed geometry device (1480 nm/60 nm). TID curves follow a similar trend for open and enclosed geometries.

4.3 Annealing effects

The annealing was done in three phases, first at low temperature for 5 days before being continued for 33 days at room temperature, followed by three annealing periods of one week at high temperature (100°C).

The variation of the current drive during annealing is presented in figure 8a, and shows that the NMOS recovery at room temperature seems to be very slow. However, the high temperature annealing (100°C for 7 days), accelerates the driving current recovery and the maximum $V_{TH}$ shift is reduced from 330 mV to 220 mV for the 240 nm/60 nm device.

Figure 8b shows that PMOS devices recover some driving capabilities even under room temperature annealing. For the narrowest devices, the transconductance degradation is reduced from the final 100% loss at 1 Grad to a 40% loss after high temperature annealing. At the same time, the current loss degradation improves from 100% to 78%. The moderate enhancement of the driving strength with respect to the transconductance recovery after annealing comes from the fact that the threshold voltage increases during the annealing period. It reaches a value of approximately 1V for the narrowest PMOS device, for which the $V_{TH}$ increase with respect to the pre-irradiation value is around 0.45 V.
Figure 8. Current drive variation with annealing (a) NMOS device (b) PMOS device.

Figure 9. Current drive variation for $V_{DS} = 1.2$ V versus the TID level for minimum size transistor (a) 120 nm/60 nm NMOS device (b) 120 nm/60 nm PMOS device.

5 Results at low temperature

5.1 Irradiation effects

The pixel detectors of ATLAS and CMS operate at low temperature. In particular, the ATLAS pixel detector has operated for phase 1 (2009–2012) at a relatively stable temperature of $-13^\circ$C except during the cooling stop periods and during pixel detector calibration scans. Irradiation tests at low temperature were therefore made in order to estimate the device degradation with TID under the foreseen pixel detectors operating conditions.

The test PCB — to which the chip was directly wire bonded — was in direct contact with a thermal chuck in which the temperature was set to $-20^\circ$C by cooling liquid flow. With this setup, the temperature of the devices was estimated to be around $-15^\circ$C. All the irradiation tests were carried out using the CERN X-ray facility with the same test set-up and in the same conditions in terms of dose rate as for the room temperature test described in section 3.1.

A comparison of the effects of high versus low temperature during irradiation at the drive current for the minimum size NMOS device is shown in figure 9a. There is in fact less degradation
at low temperature (−15°C) than at room temperature (25°C) for all tested NMOS devices and in particular for the narrowest one, for which the current drive loss is 40% for a TID of 1 Grad for low temperature irradiation, while it reaches 60% for the room temperature irradiation. The rebound (increase) observed at lower TID levels (< 100 Mrad) seems to be more important at lower temperature.

Figure 9b shows the effects of temperature during irradiation on the current drive for the minimum size PMOS device. The current drive degradation for irradiation at −15°C is limited to 60% whereas it is 100% when irradiation is carried out at room temperature.

As already observed for the room temperature irradiation, low temperature irradiation shows more degradation for the PMOS device than the NMOS device and the main part of the PMOS current drive loss is related to the transconductance degradation.

5.2 Annealing effects

The annealing phase was again done in three steps. In the first step following irradiation, the chip was placed in a freezer for 50 days at a temperature of −15°C. In the second step the device was warmed up to room temperature and monitored for 20 days. In the final step it was placed in a dry oven at 100°C for 7 days. During the entire annealing phase, the devices were biased and regularly measured.

Annealing measurements were made in the saturation region (V_{DS} = 1.2 V). Figure 10b represents the current drive variation for NMOS devices during this period of annealing and shows that NMOS devices do not recover at all.

For the PMOS devices, a slight recovery was observed even at low temperature (figure 11b). For example, the driving current loss improves from 45% to 38% for the 240 nm/60 nm PMOS device throughout the cold annealing and room temperature annealing periods. But the high temperature annealing (100°C for 7 days), strongly degrades the DC parameters, increasing the current loss from 38% to 68% for the 240 nm/60 nm device, despite the slight recovery in the transconductance factor. This degradation comes from the increase of the threshold voltage during the high temperature annealing, as was already noticed in the case of room temperature irradiated devices.

![Figure 10. NMOS devices: current drive variation as function of (a) TID level and (b) Annealing duration (measurement are shown for V_{DS} = 1.2 V).](image-url)
Figure 11. PMOS device: current drive variation at as function of (a) TID level \(T = -15^\circ\text{C}\) and (b) Annealing duration (measurement are shown for \(V_{DS} = 1.2\,\text{V}\)).

(figure 8b and section 4.3). For example for the 240 nm/60 nm device, an increase of 0.28 V with respect the pre-irradiation value of the threshold voltage is measured after a TID of 1 Grad followed by 100°C annealing.

5.3 Radiation tolerance of other 65 nm processes

In order to check whether degradations observed at high TID levels are specific to the tested process, or whether this level of damage is common to devices produced in similar submicron processes, we tested MOSFET devices in another 65 nm technology (process B). Those irradiation tests done for process B were carried out at a temperature of \(-15^\circ\text{C}\), with the same test set-up and exactly in the same test conditions than for devices issued from the process A.

In the same approach as for the process A testing, only SVT devices with different widths (120 nm, 240 nm, 480 nm and 1 \(\mu\text{m}\)) and having the minimum length of 60 nm are considered in order to estimate the effect of the width on the irradiation tolerance.

Figure 12 shows the evolution of the leakage current as a function of the TID level for NMOS devices produced in processes A and B. We can see that devices from process B have a larger leakage current increase than devices from process A and particularly for the small size devices. In fact the minimum size transistor (120 nm/60 nm) from process B shows a leakage current which increases to \(2 \times 10^4\) times the pre-irradiation value reaching a value of 40 nA for 10 Mrad TID. For wider devices the leakage current variation is less important and the maximum value reached is limited to 1 nA for 480 nm/60 nm as shown in figure 12b.

Figure 13 shows the TID effect on the current drive for minimum size NMOS and PMOS devices produced in the two processes. The minimum size NMOS device shows a larger rebound for process B devices in the region between 100 kRad and 100 Mrad. Furthermore, measurements show that the maximum rebound level decreases for wider devices. For high TID levels, the driving capability of the NMOS device decreases for process B as well as for process A. At 1 Grad, the current drive loss for the minimum size transistor is 35% for process B and 40% for process A. PMOS devices produced in process B show the same trend for the current drive variation as for process A devices and this loss is mainly due to the decrease of transconductance in both cases.
Figure 12. Leakage current as function of the TID level measured at $-15^\circ$C for $V_{DS} = 1.2$ V for processes A and B NMOS devices with W/L (a) 120 nm/60 nm and (b) 480 nm/60 nm.

Figure 13. Current drive variation for $V_{DS} = 1.2$ V versus TID level at $-15^\circ$C for minimum size transistors: (a) 120 nm/60 nm NMOS device (b) 120 nm/60 nm PMOS device.

6 Analysis and discussion

From measurements in figure 3 and figure 12, it is clear that the leakage current variation depends on the transistor width. This confirms that the primary cause of increased leakage is the reduction in threshold voltage for the parasitic STI device formed along the two edges of the device. This parasitic device also affects the current drive and the threshold voltage of the studied device and a rebound is observed for NMOS devices in the region where TID level is below 100 Mrad (figures 5, 9, 13). The maximum value of the rebound decreases for wider devices and disappears for enclosed devices. The usual explanation for this rebound is that the drain current increases first because of the charge trapped in the STI before decreasing when the interface trap density induced by the parasitic STI devices becomes predominant. This rebound is observed because the formation of the interface state is slower than the formation of the oxide charge. The rebound seems to be less important for room temperature irradiation than for low temperature irradiation. This might be explained by a reduced STI oxide charge formation for irradiation at room temperature as a fraction
of this STI oxide charge is recovered due to annealing during the irradiation. The NMOS devices show a larger rebound for the process B than for the CERN contract process (A). As for the leakage current, this is due to the influence of the parasitic STI device. We may note that this important difference between the processes for what concerns their TID tolerance observed at high dose rate should be reduced at low dose rate through the annealing effect which mainly concerns the positive charge build-up in the STI.

For TID above 100 Mrad, a strong degradation of the drive current is observed for NMOS and PMOS devices. The interface state generation at the STI/Si channel, which becomes more important than the positive STI charge, can be thought as responsible for the $V_{TH}$ shift, transconductance loss and current degradation.

For the NMOS devices, we observed only a small dependence of the degradation on the transistor width (figures 5, 10). As the effect of the STI device usually produces more important degradation in narrow devices than in wide devices, this hints to the fact that the parasitic STI device should not be considered as the unique explanation for this degradation. Additional tests and a deeper analysis need to be made in order to show if the effect of the charge build-up in the spacers present in this technology (see sketch in figure 1) could be responsible of this effect.

For the PMOS devices, degradation as a function of TID is materialized by the decrease of the carrier mobility (figures 6, 7, 11). The mobility degradation due to an increase in the interface state density at the STI/Si channel interfaces probably represents the main cause of degradation since a worsening of this effect for smaller device width is clearly observed. However, this is certainly not the only source of degradation as can be seen from the fact that the enclosed transistor also displays reduced driving strength at high TID (figure 7).

For the high TID region (TID $> 100$ Mrad), PMOS and NMOS devices show more degradation when the irradiation is carried out at room temperature compared to low temperature irradiation (figure 9). If we consider that the degradation is partially caused by the interface trap density in the STI device, we can assume that the interface trap density decreases when the irradiation temperature decreases. This makes the degradation less severe at low temperature. This is in agreement with previous work [7] where it was shown that for a decrease of the irradiation temperature, the interface trap density decreases.

High temperature annealing does not help recovering current drive, neither in the case of NMOS devices nor in the case of PMOS devices. On the contrary, performance degradation is observed after high temperature annealing for PMOS devices particularly for devices irradiated in cold conditions (figure 11b). This degradation at high temperature is somewhat counter-intuitive, but might be caused by the combined effect of irradiation and Negative Bias Temperature Instability (NBTI) as reported in [8], where devices subjects to the irradiation followed by the NBTI show a higher degradation than devices subjects to the NBTI only.

7 Conclusion

X-ray irradiation testing at room and low temperature was performed for the CERN frame contract 65 nm process expected to be used for the design of future pixel readout chips for operations in the HL-LHC context. Devices having a minimum length (60 nm) and a width varying from 120 nm to 1 $\mu$m were irradiated up to 1 Grad. Whether for room or for low temperature irradiation, the
leakage current degradation does not seem to be the main issue with this process. However, an important degradation of the drain current for both n and p channel devices starting from a dose level of about 100 Mrad was observed for the CERN frame contract 65 nm process and irradiation tests performed on another 65 nm process show similar degradation at high TID levels.

Under irradiation at room temperature, the PMOS transconductance loss is nearly 100% for narrow channel devices starting from a dose level of 600 Mrad. This turns the device off whatever the value of the gate voltage. This clearly might compromise the proper functioning of circuits, and in particular logic circuits where the size of transistors is usually set quite small.

Irradiation tests at low temperature show less degradation than at room temperature. In fact, the current drive degradation under irradiation at $-15^\circ C$ is limited to 60%, whereas this reaches 100% when radiation is conducted at room temperature, which is an interesting feature in view of the low-temperature environment of LHC experiments.

For the NMOS devices, no substantial drive capability could be recovered in any of the three stages of annealing described in the paper. However, a little recovery is observed for PMOS devices at low temperature, particularly at the beginning of the annealing period. But when the annealing was carried out at high temperature (100°C) for the PMOS devices irradiated either at room or at low temperature, we observed rapid and strong degradation in DC parameters, resulting in a significant increase of the threshold voltage.

These presented results are from the first irradiation tests performed with X-ray to a dose level of 1 Grad. Consequently some aspects of device behavior are not yet well understood and need to be further studied. This work will be continued within the RD53 collaboration in order to check the reproducibility of the X-ray test results on other samples, and to understand discrepancies with other test results obtained with $^{60}$Co or 3 MeV proton radiation sources, or discrepancies noticed in device recovery depending on bias conditions.

It can be noted that some basic test circuits were already designed with the 65 nm process and showed degradations for high TID levels. A ring oscillator stage was irradiated up to 200 Mrad [4] and has shown a frequency decrease because of the reduction of drive current of the inverter’s PMOS. Thus a speed reduction with accumulated TID can be foreseen for digital circuits.

For a pixel detector chip designed for the ATLAS and CMS experiments, a speed reduction for digital circuits can be accepted if known and quantified at design time. The digital synthesis tool can be used to put significant timing margins. A large majority of the pixel chip logic only needs to run at modest speed (40MHz) and only few fast speed circuits (e.g. readout link serializers) will need to take dedicated precautions for significant speed degradation from radiation.

Some design techniques consisting of using relatively large size or enclosed geometry devices can also be adopted in analog circuits to reduce the effects of irradiations.

High leakage currents would be detrimental in particular for the power consumption of the pixel detector chip but this seems not an issue for the CERN contract 65 nm process.

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