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THE ALEPH SILICON VERTEX DETECTOR

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presented by Ettore Focardi

- 1- CERN, Geneva Switzerland
- 2- INFN, University and Scuola Normale Pisa, INFN and
University of Florence, University of Naples, Italy
- 3- MPI and TU Munich, FIMS Duisburg, Germany
- 4- University of Wisconsin, USA

ABSTRACT

The Aleph silicon vertex detector at the LEP e^+e^- collider at CERN is described. A detailed information on the various components of the detector is given. Preliminary results obtained during 1990 LEP running are presented.

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2. SYSTEM OVERVIEW

1. INTRODUCTION

The identification of heavy quarks and leptons by tagging decay vertices among the collision products of e^+e^- interactions has developed rapidly in the past ten years. Different generations of vertex detectors have been built: even with a resolution on impact parameter greater than 100 μm , experiments at e^+e^- storage rings (PEP, PETRA), have demonstrated that vertex detectors can enhance the sensitivity in the detection of heavy leptons and quarks. A silicon vertex detector with an improved resolution will provide a high precision measurement of charged tracks close to the interaction point and this will complement the momentum measurement in the main tracking chambers. It will allow for the measurements of multiple vertices, separation of charm and beauty decays from light quark background events, and the measurement of lifetimes of short-living particles with decay times $\geq 10^{-13}$ sec.

The Aleph minivertex detector (ref 1), is made out of two concentric barrels of double sided Si microstrip detectors positioned around the beam pipe. The detector was separated in three sectors to allow a late installation when the Aleph detector was already in the beam line. Each sector has been slid in from the outside, by using a pulling string system, to a precise position on a carbon fiber tube 300 μm thick, 1 m long that was already mounted onto the Al beam pipe (400 μm thick); precision pins held the three sectors in the final position. Each sector (fig.1), 300 mm long, was made out of two flanges, 4 mm thick, and 5 carbon fiber tubes 8 mm in diameter, 0.2 mm thick. The flanges were precisely machined to allow a face positioning within 10 μm . The electronics is cooled by air flowing through holes in the tubes. A composite structure Al (25 μm) + carbon fiber (125 μm thick) was used for inner and outer cover as electrical and mechanical shielding.

Fig.1 One of the three sectors.

Each sector was designed to accommodate 4 'faces' in the inner layer at an average radius of 9.6 cm and 5 'faces' in the outer layer at an average radius of 11.2 cm. The total number of 'faces' is 27. One 'module', (fig.2), is the elementary unit of the detector, two modules glued together make one 'face', fig.3.

19 'faces' have been installed in Aleph for 1990 LEP run (fig.4): the complete inner layer (12 faces) plus 7/15 of the outer layer, with a total of 58K analog channels. To reduce the number of output lines a multiplexing of 1:256 was used.

Fig.2 R-phi side view of one module.

Fig.3 Sketch of one face: top, r-phi view up, bottom, r-z view up

Fig.4 Faces installed in Aleph for LEP run 1990.

3. DETECTOR 'MODULES'

One detector 'module' consists of 2 Si detectors $51.2 \times 51.2 \text{ mm}^2$, $300 \mu\text{m}$ thick with strips on both sides, plus two ceramics, both $250 \mu\text{m}$ thick, used as mechanical support for Si detectors and as substrate for thick film hybrid circuitry to accommodate the front-end electronics for readout. Two types of double sided silicon strip detectors have been installed, the main difference being in the coupling of the strips to the front-end electronics: both designs are based on AC coupling between the silicon detector and the preamplifiers but one (MPI type) has the AC coupling capacitors built directly onto the Si wafers, while the other (Pisa type) needs separate capacitor chips. A detailed description of the Si detectors is given in ref.2),3). The Si detector geometry is the following:

- junction side (r-phi projection)
strip pitch $25 \mu\text{m}$, readout pitch $100 \mu\text{m}$
  - ohmic side (r-z projection)
strip pitch $50 \mu\text{m}$, readout pitch $100 \mu\text{m}$ or $200 \mu\text{m}$
- The detectors within a module have their strips daisy chained on the junction side.

4. FRONT-END ELECTRONICS

The thick film hybrids(ref.4)in each module have as active components several custom designed CMOS chips: a charge sensitive amplifier with 64 channels/chip (CAMEX 64A), a steering chip which produces the timing sequence for the readout and a 'line driver' that drives differential outputs into a 100Ω twisted pair cable. The preamplifier chip, CAMEX64A (ref.5), with a readout pitch of $100 \mu\text{m}$, provides signal amplification, noise filtering, parallel storage and serial readout of the analog signals. Fig. 5 shows a schematics of one channel.

Switched capacitor filters are used to reduce the noise by multi-correlated double sampling. Table 1 shows the main parameters of this chip. The 256 analog signals from 4 readout chips are fed into the custom designed line driver that has an adjustable gain and provides differential output.

Fig.5 CAMEX 64A single channel schematics.

To minimize the amount of cable connections to the module the digital steering chip has been designed in CMOS technology that upon a receipt of two input lines (initialize pulse and a pulse train) provides all eighteen switching pulses necessary to operate the CAMEX 64A. TTL logic levels are used for input and output. A block diagram of the readout scheme is shown in fig.6.

Fig.6 Readout scheme block diagram.

Table 1- The parameters of the CAMEX64A.

CAMEX 64A	
Parameter	Value
Number of channels	64
supply voltage	± 5 V
Charge Sensitive Amplifier Section	
Open loop voltage gain	70 dB
Feedback capacitor	≈ 0.3 pF
Rise time	70 nsec
Fall time	80 nsec
Readout Section	
power consumption/channel	<2 mW
Charge amplification/channel	15 mW/IC
Gain error	<0.6 %
Sampling time (4 samples)	min. 500 ns
Output readout time	min. 300 ns
Noise performance at 1 μ sec sampling time	
Noise charge (e-)	ENC=335+30 $\cdot$ Cin (pF)

5. PERIPHERAL ELECTRONICS

There are three categories of signals needed or provided by each module: power (low, high voltage) and detector bias voltage, digital and analog clocking and analog outputs. Fig.7 shows a sketch of the connections between the modules and the peripheral electronics.

The preamplifier chips need 3 voltages referred to a common ground, GNDL: VDDL (+5 Volt), VSSL (-5 Volt), VrefL (the reference voltage that regulates the power consumption). Since the electronics on the detector high voltage side (ohmic side) is referred to the detector bias voltage GNDH, a different set of three voltages is used to power the chips on this side (VDDH, VSSH, VrefH). Vref=0 has been chosen during the operation, giving a power consumption of 1 W/module.

In the detector low and high voltage side there is a provision for a 'guard ring' voltage which allows to vary the detector bias voltage with respect to the ground reference voltages for the readout electronics.

Fig.7 Connections between modules and peripheral electronics.

The clocking signals are divided into analog and digital signals: the analog signals are calibration signals for the charge sensitive preamplifiers; the digital signals are a reset pulse and a pulse train for the steering chip which provide the CAMEX64A and the line drivers with all the clocking signals necessary for their operation.

Finally each detector module has 6 outputs each of them transmitting a sequence of 256 analog voltage levels, corresponding to the multiplexed output signals of four CAMEX chips. All of these signals are fed into the detector in the following way:

- power and bias voltages are supplied by computer controlled modules developed by LABEN (Milano) to match the requirements; with this unit a suitable sequence for turning ON and OFF the voltages in the detector module can be programmed; the signals are fed into a special fan-out card (AFAC).
- the clocking signals provided by a custom made Fastbus unit (MVDRCU) are multiplexed and fed into the AFAC.
- the output signals routed to several 8-bit flash ADC (TPD).

An adapter card (ADAC) is used for all of these signals.

Fig.8 Residuals distribution for r- ϕ projection.

Fig.9 Residuals distribution for r-z projection.

6. PRELIMINARY RESULTS

Before the installation in the Aleph experiment some modules were put in a test beam at the Cern SPS and a measurement of the spatial resolution was performed. As preliminary result a resolution of $12\ \mu\text{m}$ in the r- ϕ projection, where the readout pitch is $100\ \mu\text{m}$ (fig.8) was obtained. In the r-z projection, for a readout pitch of $200\ \mu\text{m}$ the corresponding resolution was $24\ \mu\text{m}$ (fig.9). Since March 1990 the Si vertex detector is taking data in the Aleph experiment.

Fig.10 Hadronic event in the ALEPH apparatus with the corresponding view in the vertex detector.

Fig.10 shows an event in the Aleph apparatus with the corresponding view in the vertex detector. Fig 11 shows the strips fired in one module with the corresponding pulse height in the r- ϕ and r-z projection and the extrapolated point from the tracking system, before the alignment. A signal to noise ratio of 1:12 was measured in agreement with the value obtained in the test beam.

RUN: 7418 / EVENT: 26

1 Phi hits, 1 Z hits

Fig.11 Fired strips in one module with pulse heights in the two projections. The large ellipse is the expected impact point of the track as projected from the tracking system.

7. CONCLUSION

A new kind of vertex detector is now collecting data in the Aleph experiment at Cern in the LEP collider. The fact of having a high density of readout elements on both sides of the silicon wafers makes this detector unique and able to give very precise spatial measurements of tracks coming from e^+e^- collisions; heavy flavours decays can then be tagged by looking for secondary vertices.

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