The "V" bus family, FUTUREBUS+ and SCSI.


Abstract

The ECFA working group on buses was initiated with the task of reviewing the present and short term future situation regarding the standards for buses with a view to making recommendations on the suitability of their use in a general LHC data acquisition system. This report treats the VMEbus, VSB, VX1bus, VICbus, FUTUREBUS+ and SCSI buses.

Introduction

In the general design of a data acquisition system there is a requirement for four varieties of bus, the system bus, the sub-system bus, the cable or interconnect bus and the peripheral bus. A data acquisition system is composed of functional modules which will typically be micro-processor systems with specific tasks within the overall system. The micro-processor systems physically take the form of a 19 inch rack mounting "crates" and are interconnected by either point-to-point links or an interconnect bus. An interconnect bus is chosen if information available to several systems must be shared between them for example in trigger processing or event building. The boards forming a particular "system" within a crate are connected by the system bus which provides inter-board communication and resources such as clocks and power supplies. Both VMEbus and FUTUREBUS+ are specifications for system buses. The physical format of the bus is one or more rigid backplanes extending the width of the crate. The electronic characteristics of the backplane limit the rate at which information can be distributed between boards to of the order of one hundred million transfers per second. A high data transfer rate can be obtained by transferring several bytes in parallel. The VMEbus has a maximum word width of 32bits (extendible to 64-bits in the latest revision which allows multiplexed
transfers) while for FUTUREBUS+ this value is 256-bits. The data transfer rate for FUTUREBUS+ is of the order of 1 G.byte.S⁻¹ so that FUTUREBUS+ is to be recommended where high data transfer rates are required. In some situations, for example trigger processing, it is necessary to connect devices with requirements which are outside the bus specification for example ECL logic or analogue electronics. The VXI bus is an extension to the VMEbus specification which provides standard mechanisms for additional power supplies, well defined analogue and digital signal paths, and RF shielding and so on.

Within a system, because of the finite bandwidth of the system bus it is often necessary to connect two or more boards without resorting to use of the system bus. The VSBbus is a sub-system bus for VMEbus systems which allows the sub-grouping of boards within a VMEbus system.

The SCSI bus is a peripheral bus which provides a mechanism for connecting commercially available "standard" peripherals such as printers, disks and tapes to a system. It is included here for completeness. The detailed characteristics of the buses treated here is treated in detail elsewhere.[1]

The VMEbus.

The VMEbus specification IEEE-1014 has been extremely successful and is widely accepted commercially. The number of VMEbus manufacturers is numbered in the hundreds and the products in the thousands. VMEbus has for many years been one of the highest performance buses for the construction of modular computer systems. This reason and the commercial availability of modules has lead to its use in many high energy physics experiments.

A VMEbus system consists of up to 21 modules in a 19 inch rack mounting crate. The bus is implemented using two 96 way backplanes one of which provides the minimal 16-bit bus with 24-bit addressing while the second provides extension to 32-bit data and address. The second backplane also provides 64 connector pins which are not covered by the specification and are free for user definition or use by the VSBbus. For a 32-bit implementation most bus masters commonly used support block transfer rates of around 10-20 M.Byte.S⁻¹. The bus
supports multiple masters on three priority levels and a seven levels of interrupt. Block transfers are supported. The VMEbus specification does not provide high level guide-lines on how to implement a system, such as inter-processor communication and error recovery protocols. The power supply specifications for VMEbus do not easily support analogue or ECL logic on a board.

The VSBbus.

The VSBbus is a sub-system bus designed solely to complement VMEbus, it uses the 64 user definable pins of the VMEbus P2 connector and takes the form of a rigid backplane with between 2 and 6 connectors which plugs onto the back of the VMEbus P2 backplane. The bus provides 32-bit multiplexed address and data, it supports multiple bus masters, interrupts and block transfers. As a complement to VMEbus the VSBbus is well matched in performance. The drawbacks of the bus are those of the VMEbus, a lack of system level specification and the board size limit.

The VXIbus.

The VXIbus is a specification for an instrumentation bus which uses the VMEbus specification as a basis. Four board formats are specified. Formats A and B are equivalent to the VMEbus specification for 16 and 32-bit modules, in the case of format B the 64 user definable pins of the VMEbus are completely specified by VXIbus as additional power supplies, clocks, analogue and digital lines. Format C extends the boards area of format B by lengthening the board from 6.3 to 9.2 inches. With format D a third backplane is added and the board size is increased to 14.4 by 13.4 inches. The VXIbus slot width for formats C and D is 1.2 inches (compared with 0.8 for VMEbus) which allows for electromagnetic screening between boards. The VXIbus specification allows commercial VMEbus boards to be used if they do not make any assignments to the outer rows of pins of the P2 connector.

VXIbus is in use in nuclear physics, commercial and military applications were the large board size and provision for ECL and low level analogue signals make it an ideal instrumentation bus. VXI was intended as a successor to GPIB and is rapidly gaining popularity.

The VICbus.

The VICbus is a specification for an interconnect bus for use with buses such as
VMEbus. Interfaces to several buses have been implemented so that a mixed system can be implemented. Physically VICbus is a cable bus with several systems connected at intervals along the cable by master or slave interfaces. It provides 32-bit memory mapped or buffered transfers between tested at a rate of 3 M.Byte.S⁻¹. Multiple masters are allowed and interrupts can be transmitted by slave interface to the master.

VICbus is a true bus allowing transparent memory mapped transfers between up to 31 devices on cables up to 100m long.

FUTUREBUS+.

FUTUREBUS+ is a specification, in an advanced stage of preparation, for a system bus. A specification for an interconnect bus is being prepared. The bus will support the technology which it is expected will be developed by the start of the 21st century but can be realised now. The backplane system bus suffers from the usual theoretical transfer rate limitations but by allowing a scalable data word size of up to 256-bits in parallel it is possible for 2.3G.Byte.S⁻¹ transfer rates to be realised with currently available technology. The bus contains specifications for multiple bus masters, interrupt handling as well as specifications for high level system features such as cache coherence across the bus.

The first FUTUREBUS+ products are to be expected by the end of 1991 which is within the timescale of any LHC projects. The draft specification for the bus is already available. Its expected characteristics put FUTUREBUS+ in the performance range which can handle the main data stream from an LHC experiment. The specification of a high speed interconnect bus would allow FUTUREBUS+ to be used in areas such as the event builder where a high degree of connectivity is required.

SCSI.

SCSI, small computer system interface, is designed to provide access to peripherals such as tape and disk drives, printers and so on. It is the most widely used interface for personal computers and workstations but is becoming increasingly used in data acquisition. Cartridge tape drive systems driven from VMEbus via a SCSI interface are available which will handle rates of 3-4 M.bytes.S⁻¹. An update to the specification provides for either an increased word width and/or improved protocol to increase throughput. A
system of several tapes writing in parallel could be implemented with current technology to handle the expected data rate for an LHC experiment. It is likely that a system of this type will be used to provide data logging in LHC experiments.

CONCLUSIONS.

The ECFABUS working group has proposed a simple standard model for a LHC data acquisition system. (2) Based upon these assumptions an estimate of the usefulness of the bus standards described here can be made.

The data transfer rate for VMEbus although adequate for applications in current generation experiments is an order of magnitude too low for VMEbus to be used in the main data stream of a typical LHC experiment. The extension to 64-bits goes some way to relieving this problem but VMEbus still falls short in performance. The VMEbus could still find uses in the data acquisition at those points where the more performant but also more expensive systems would not be required, in particular the monitoring of data samples, control and data logging. However, VMEbus still has a role to play since it is cheap and widely available it is likely that it will be used for medium speed data acquisition, for example monitoring and on-line event analysis where only a sample of the data stream is treated. VMEbus may also have a valuable role to play in control of the overall system and downloading of software especially as the internal bus of workstations.

In a LHC environment VXIbus could perhaps find application in the trigger where the availability of a large board area, ECL supplies and bus lines would be useful. As an instrumentation bus VXIbus could find an application in what is currently called slow control. In LHC it will be necessary to provide information on hardware failure in real time to allow for dynamic reconfiguration without stopping data taking. By the time the first LHC experiment comes on line FUTUREBUS+ will be able to provide the required performance for handling the main data stream. It is also likely that FUTUREBUS+ hardware will be available during the early planning stage when prototypes are required. However the cost of FUTUREBUS+ hardware may mean that at stages where massive parallelism is required a different solution will be required.
Finally it is likely that the data from a LHC experiment will be recorded on a high speed recording medium by drives interfaced via SCSI bus to dedicated VMEbus or FUTUREBUS+ data logging systems.

Acknowledgements

The content of this document is the result of a collaborative effort on behalf of the members of the ECFABUS working groups.

References

[1] "Summary of backplane bus characteristics", Editor C.F.Parkman, (to be published by the CSI group), and references therein.