LHCb Upstream Tracker
Marina Artuso, SYRACUSE UNIVERSITY
for the LHCb UT working group

Abstract
The detector for the LHCb upgrade is designed for 40 MHz readout, allowing the experiment to run at an instantaneous luminosity of $2 \times 10^{33} \text{cm}^{-2}\text{s}^{-1}$. The upgrade of the tracker subsystem in front of the dipole magnet, the Upstream Tracker, is crucial for charged track reconstruction and fast trigger decisions based on a tracking algorithm involving also vertex detector information. The detector consists of 4 planes with a total area of about 8.5 m², made of single sided silicon strip sensors read out by a novel custom-made ASIC (SALT). Details on the performance of prototype sensors, front-end electronics, near-detector electronics and mechanical components are presented.

The Upstream Tracker

- The UT consists of four planes of silicon sensors, and has significantly less material in the forward region than the current Si tracker.
- The first and last planes have strips oriented vertically, and the middle two are at rotated by $+5^\circ$ and $-5^\circ$.
- Near detector electronics provides needed interfaces to DAQ system in the control room.

High efficiency, low ghost rate, and fast speed of the Velo-UT track-finding make it possible to reconstruct all tracks of interest at the full 40 MHz rate of the LHC.

Mechanics and cooling

The UT stave (1.2 m x 10 cm) provides a stiff, low mass core on which the sensors, hybrids and readout cables are mounted. It also provides active cooling with an evaporative CO₂ system. Silicon-SALT hybrid modules are mounted on both sides of the staves to provide full coverage in the LHCb acceptance. The first two full-size staves have been produced.

Silicon micro-strip sensor

- The majority of the detector will consist of 10x10 cm² p*-in-n sensors with 512 read-out strips (Type A) with ~190 μm pitch.
- Embedded pitch adapters to match strip pitch with front-end electronics readout pitch.
- Possibility of top-side bias through n+ peripheral implant.

Dedicated front-end electronics (SALT)

Dedicated radiation-hard front-end ASIC (SALT) features PA-shaper with fast return to the baseline, 6-bit ADC, complex digital processing.

Flex cables and near-detector electronics

- Flex cables provide data/monitoring interconnection and power distribution.
- SALT powered with rad-hard linear regulators 10 μA away.
- SALT output data integrity (SILVS) and interface with flex cable validated.

96 e-links sending synchronous ascending pattern Eye Height: 325 mV
Eye Width: 2.19 μs

TFC signals without flex cable
TFC signals with flex cable between source and hybrid