Development of ATLAS Liquid Argon Calorimeter Readout Electronics for the HL-LHC

Andy Tiankuan Liu
on behalf of
the ATLAS LAr Collaboration
Outline

1. Introduction
2. Front-end analog
   – 65 nm
   – 130 nm
   – SiGe
3. ADCs
4. Optical links
   – Laser driver array ASICs
   – Optical transmitter array module
5. Summary

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ATLAS LAr Detector and Phase-II Upgrade

LAr Detector @ 87K (Cold)
Will not change

Functionally the Same as the current detector

New Approach:
Digitize and ship all Digital Data
@ 40 or 80Msps 14 bits  2 Gain Stages

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Upgrade Objectives

- Detector capacitance 0.2 to 1.5 nF
- Noise requirements ~ 100 nA
- Signal dynamic range ~ 16 bits
- Moderate radiation tolerance requirements ~300 krad, $10^{13}$ n/cm$^2$ 1-MeV eq. neutrons
- Selectable Input impedance 25 or 50 Ω (+/-1.5%) to provide cable termination
- Digitize all 128 channels/FEB 14 bits, 2 gain scales @ 40 or 80Msps.
- Ship data from all channels off detector (trigger-less readout).
- Keep the power dissipation to the current one or lower.
Options Being Explored

1. Multi-ASIC/technology solutions
   - Preamplifier + shaper
   - ADC
   - Encoder + serializer
   - Laser drivers and optical transmitters

2. One ASIC System-on-a-Chip Solution
   - Preamplifier + shaper + ADC + serializer
     (collaborative Investigations by BNL, Penn, Omega/LAL, Nevis, and SMU)
   - Laser drivers and optical transmitters
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Front-End System On Chip

- FESOC (front-end system on a chip): BNL motivated and proposed
- 8 Front-end channels
  - Dual range
  - Programmable gain
  - Programmable termination
  - Programmable filter
  - 4x and 8x sum
- To be integrated with ADCs and mux/encoder/serializers
- Power dissipation ~1.2 W
- CMOS 65 nm

HLC1: 8-ch. analog FE ASIC

Slide content from Gianluigi De Geronimo, LAr Week, June, 2016
Preamp in 65 nm - Design

- New concept
- Fully differential amplifier with passive feedback
- Very stable termination (R and N independent of signal current)

\[ v_i = -\frac{v_o}{N} \]

- **R-noise** \(4kT/R\)
- **Input impedance** \(+R/(N+1)\)

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Preamp in 65 nm - Performance

- ENI ~57nA rms at 260pF, 40ns
- Linearity now within 0.1% at 9mA, within 0.5% at 10mA
- Power dissipation ~ 100mW/ch. from single 1.2V supply
- The layout design is being finalized, and the chip submission is imminent.
FE Analog in 130 nm - Design

Line termination

\[ Z_{in \, PA} = \frac{R_0 + Z_{in \, (SCB)}}{1 + |G|} \]

Noise

\[ \frac{4kTR_0}{(1 + |G|)^2} \]

<table>
<thead>
<tr>
<th></th>
<th>50 Ω</th>
<th>25 Ω</th>
</tr>
</thead>
<tbody>
<tr>
<td>R0</td>
<td>500 Ω</td>
<td>100 Ω</td>
</tr>
<tr>
<td>G</td>
<td>C1/C2=9</td>
<td>C1/C2=3</td>
</tr>
<tr>
<td>Noise</td>
<td>5 Ω</td>
<td>6 Ω</td>
</tr>
<tr>
<td>Dynamic</td>
<td>2 mA with Rf=5kΩ</td>
<td>10 mA with Rf=1kΩ</td>
</tr>
</tbody>
</table>

Slide content from Laruent Serin (Omega/LAL) ACES presentation March 8, 2016
FE Analog in 130 nm - Performance

- 25.5Ω @ 1 MHz
- Impedance flat from 10 kHz to 100 MHz
- < 1 Ω variation versus current due to Super Common base Zin variation
- Noise dominated by R0 and NMOS ampli: 150 nA with 1.5 nF

Frequency (Hz)

Input impedance (Ω)

High gain (0-1-mA) ±0.2%

Low gain (1-10 mA) ±0.2%

Integral nonlinearity with CR-RC2 (40 ns peaking time)
FE analog in 130 nm - Prototype

- Super Common Base type Preamp
- Programmable Zin 25 or 50Ω
- 2 Gain Ranges 2 or 10mA
- Input Noise eq. < 10Ω
- High current Saturation mitigation
- Preamp Pwr 7mA @ 2.5V ~ 18mW

BNL/Omega/LAL Collaborative effort
- Test boards/benches similar
- Comparative meas. of 65/130 nm chips

Goal -
Converge to common CMOS preamp architecture technology.
FE Analog in SiGe (180 nm)

- Similar to the current design which is implemented with discrete components
- Bonding option for 25/50 Ω. No impedance/dynamic range tuning
- Might be marginal at High frequency (> 30 MHz) and large current
- Good noise performance on simulation: 25 Ω preamp: 86 mW, 97 nA for 1.0 nF with CR-RC2 shaping
- Layout is existing but no submission date known... mainly funding issue
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ADC in - Specs

- High resolution: 14 bits
- High speed: 40-80 MS/s
- Low power, small area
- Radiation-tolerant
Chip Architecture

- The work is still “in-progress” and the chip FEB2 context study started
- 65 nm CMOS
- 8-channel 14-bit ADCs at 40 MSps
- Outputs serialized at 320 MHz (DDR)
- QFN package preferred (100 pins, 0.5 mm pitch, 12 mm x 12 mm)
Possible Layout

Power cuts

Analog side

Digital side

ADC channels (DRE and SAR). Silicon space 0.2 x 1mm per channel

References

• Chip produces data volume of 5.12 Gbit/s
• Die size 1.98 x 1.95 mm
• 136 die I/O pads
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Laser Array Drivers: Overview

• SMU is a member of IpGBT collaboration led by CERN. IpGBT is based on a 65-nm CMOS technology. The mux, encoder and serializer, major parts of IpGBT, will be integrated with the front-end analog and ADCs.

• SMU is a member of Versatile Link + collaboration led by CERN. SMU is designing laser array drivers and optical transmitter modules.

• VLAD (VCSEL Array Driver) and IpVLAD (low-power VCSEL Array Driver) are 4-channel, 10-Gbps-per-channel VCSEL array driver ASICs designed in a 65-nm CMOS technology with different output structures. Both drivers receive low-swing CML 400 mV<sub>p-p</sub> signals compatible with IpGBT output.

1. Talk: Csaba Soos, Versatile Link PLUS Transceiver Development, 11:10 AM, Thursday.

Tiankuan Liu, TWEPP, Karlsruhe, Germany, September 27, 2016
Laser Driver Array: Design and Layout

1.7 mm

1.9 mm

Pitch 0.25 mm

Two-stage pre-driver

VLAD output driver

IpVLAD output driver

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Laser Driver Array: Optical multi-channel test Results

- Total jitter = 48 ps
- Total power consumption 33.9 mW/ch
- Total jitter 35 ps
- Total power consumption 21.6 mW/ch. This is a world record now.

- VLAD, 10 Gbps optical eye with adjacent channel working simultaneously
  - Output: 3.5 mA ~ 7.5 mA,
  - Input: diff p-p 400 mV PRBS 7

- IpVLAD, optical, 10 Gbps optical eye with adjacent channel working simultaneously
  - Output: 1.7 mA ~ 6.3 mA
  - Input: diff p-p 400 mV PRBS 7
**Laser Driver Array: Module Development**

- **ATx (Array optical Transmitter)** is a 12-channel optical transmitter module developed at SMU, based on the MOI/LTP from US Connec and the AZ8 connector from Samtec with custom active-alignment method for the module assembly.
- **ATx** is used as a test vehicle for VLAD/lpVLAD.

**ATx footprint:** 10 mm x 15 mm. MOI with a Prizm connect to a 12-way fiber ribbon.

The base will be reduced from 2 mm to 1.2 mm. ATx modules will be 5.3 mm tall for now. In the final design we hope to reduce the height to 4.5 mm.
Summary

• The ATLAS LAr front-end readout electronics without trigger is under development to meet the high luminosity requirements.

• An approach of System-On-Chip is being targeted: integrating all front-end functional blocks (preamplifiers/shapers/ADCs/mux/encoders/serializers).

• Three front-end analog ASICs in early development stages show promising performances within termination, ranging capacitance range, input signal dynamic range and power requirements.

• New ADC design has been started.

• Two radiation-tolerant laser driver array ASICs and an optical transmitter modules are prototyped and tested.