SALT Readout ASIC for Upstream Tracker in the Upgraded LHCb Experiment

Krzysztof Świentek
on behalf of LHCb UT collaboration

Faculty of Physics and Applied Computer Science
AGH University of Science and Technology

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Outline

• Introduction

• SALT design

• Tests of prototypes
Introduction
Upgrade of LHCb Inner Tracker at LHC

- Upstream Tracker (UT) replaces the Tracker Turicensis (TT)
- 500,000 silicon strip detector channels
- Readout frequency increases to 40 MHz – *currently Level-0 trigger is limited to 1MHz*
- No hardware trigger in UT only software one
- A data packet is created for each BX – better control
- New readout electronics is needed!
Introduction
Readout of UT silicon strip detectors

- 4 sensor types (250 um thick)
  - $p^+$-in-$n$, 10 cm, pitch 190 um
  - $n^+$-in-$p$, 10/5 cm, pitch 95 um
- ~900 hybrids with 4 or 8 ASICs

- ~3900 128-channel readout ASICs – SALT
- Data stream depends on position – different number of active e-links in SALT
Introduction
The goal and short history

The Goal – SALT readout ASIC for UT detector

AGH-UST Design team:
- staff: M. Firlej, T. Fiutowski, M. Idzik, J. Moroń, K. Świentek
- PhD students: Sz. Bugiel, R. Dasgupta, M. Kopeć, M. Kuczyńska

SALT story in short:
- Two submissions (5 ASICs) of key functional blocks (Preamplifier&Shaper, Single-to-Diff converter, 6-bit ADC, SLVS, PLL, DLL) done in IBM CMOS 130 nm - designed&fabricated and mostly tested
- In 2014 collaboration decided to move to TSMC CMOS 130 nm
- In February 2015 a large submission – 8 chips, including SALT8 and various blocks, were submitted in TSMC 130 nm – partially tested, problems with ESD/pads (mainly FE and ADC chips)
- In November 2015 SALT8 version 2, 8-channel FE&ADC chips plus other blocks (e.g. bandgaps) submitted, just fabricated, tested by JC
- In June 2016 complete 128-channel SALT chip was submitted
Introduction
SALT specification

- CMOS 130 nm technology
- 128 channels, Front-end & ADC in each channel
- Sensor: capacitance 5–20 pF, AC coupled
- Both input signal polarities ($p^+$-in-$n$ and $n^+$-in-$p$)
- Input charge range ~30ke–
- Noise: ENC ~1000e– @10pF + 50e–/pF
- Pulse shape: $T_{\text{peak}}$ ~25 ns, very short tail: ~5% after 2*$T_{\text{peak}}$
- Crosstalk < 5%
- ADC: 6-bit resolution (5-bit/polarity), 40MS/s
- DSP functions: pedestal and common mode subtraction, zero-suppression
- Serialization & Data transmission: 320 Mbps e-links to GBT, SLVS I/O
- Slow control: I2C
- Power < 6 mW/channel
- Radiation hardness ~30 MRad
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SALT – Silicon ASIC for LHCb Tracking Architecture

- Front-end & ADC in each channel
- Advanced Digital Signal Processing (DSP)
- and many other features blocks: PLL, DLL, TFC, I2C, SLVS, ...
SALT design
Preamplifier and Shaper

- Charge sensitive amplifier (Krummenacher for DC output)
- 3-stage shaper (complex poles and zeros) gives the requested pulse with short tail
- Common mode (vcm) is kept at half power supply to work with both pulse polarities
- Power consumption: ~1.2 mW
Main features:

- SAR architecture, 6-bit resolution
- 40 MSps nominal sampling rate
- Merge Capacitor Switching (MCS)
- Capacitive DAC with 3b/2b split
- Dynamic comparator
- Dynamic asynchronous logic
- Bootstrapped input switches
- Power consumption $\sim 350\mu W$
SALT design
PLL, DLL

PLL features:
- High frequency (160MHz) clock for serializer
- Input frequency 40 MHz
- Power consumption ~0.5mW at 160MHz
- Multiplexing – 2 output phases selected from 16 uniform phases (DDR deserialization)

DLL features:
- ADC sampling phase setting
- Input frequency 40 MHz
- Power consumption ~0.7mW
- Multiplexing – 1 output phase selected from 64 uniform phases
SALT design
DSP operations

- ADC output is synchronized via async FIFO
- Input data: 6 bits (5 bits plus sign)
- Noisy or dead channels can be masked
- All channel values can be inverted (1 config bit)
- Pedestal subtraction – subtraction in each channel with different value
- MCMS – Mean Common Mode Suppression
  - sum of channels below threshold
  - division by number of channels – average
  - subtraction in each channel
- ZS – Zero suppression
  - only channels above threshold are sent out
SALT Design

TFC commands in data processing

- Data chain is a pipeline
- Timing and Fast Control (TFC) byte every clock cycle – up to 8 commands
  - Calib generates a test pulse
  - NZS generates data packet without ZS – for debugging
  - HeaderOnly & BxVeto generate the smallest packet HEADER
  - Synch – SYNCH packet for readout synchronisation
SALT design
Verification of digital part

- Extensive checks of full design functionality
- High level of abstraction – object oriented language SystemVerilog
- UVM (Universal Verification Methodology) – verification library&methodology
- Each interface has its own agent
  - driver converts transaction to signals
  - monitor converts signals to transaction
- Self-checking verification based on constrained random data stimulus

Example of DSP verification
Serializer and other modules are verified analogously
SALT Design
Floorplan and layout

4095um x 10900um

Top/bottom pads only for wafer screening

64 channels
(FE+S2D+ADC)

Digital
(DSP
+mem
+serial
+I2C
+PLL
+DLL)

128 inputs

common bias
& monitors

64 channels
(FE+S2D+ADC)

Digital sup.

Analogue supply

& Fast signals

& Slow signals

Only left & right sides bonded to the hybrid.
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Tests of prototypes
Key functional blocks

• Operation of all key blocks (Front-end, ADC, PLL, DLL, Bandgap) was positively verified for CMOS IBM 130 nm & TSMC 130nm prototypes

• SALT8 version 1 was functional, whole readout chain was tested, some issues in analogue and digital parts were found and corrected in SALT8 version 2

• SALT8 version 2 – almost all requested functions implemented, functional tests finished

• SALT (SALT128) – delivered, but not tested yet
Tests of prototypes
Layout of SALT8

Analog & Mixed Mode  2.8 x 1.19 mm²  Digital part
Mean common mode (MCM) is an average over channels without signal.

NZS event packet includes MCM & the number of channels used in the calculation.

SALT8 was configured specially to achieve large MCM range for test purpose.

MCM from offline calculation are consistent with SALT8 calculation.
Tests of prototypes
SALT8 trim DACs and test pulse

- The fact that we see the expected signals at the SALT8 output, when applying input signal, means that the whole multi-channel (8) chain (front-end, single-to-differential, ADC, digital processing) works well.

- Front-end pulse can't be observed directly:
  - collecting NZS data packets
  - each point is an average from several hundred measurements
  - delay controlled via SALT8 configuration

![Graph showing signal baseline and Trim DAC value relationship](image)

![Graph showing ADC pedestal and time offset](image)

*Q ~ 2 MIPs in 250 µm Si*

*Chan 7 is not connected to injection connector*
Tests of prototypes
Pulse shape using laser source

Q ~ 1
MIPs
Primary channel
Share, induced, coupling
Coupling

- Laser beam of ~7 ns width.
- The laser beam is centred on strip connected to channel 4, ~20 mm from the border of strips.
- For long strips crosstalk is around 5% as in specs.
- In each of 8 runs, laser beam is centered on strips one by one.
- Collection of pulse shapes from all channels that are hit by laser beam in each run.
Simulation of full SALT

• Post layout simulation with sensor model
• An input pulse send to every second channel – 64 channels active
• The shape of output pulse is correct
• The sensor coupling is clearly seen in channels without input signal as in measurements
Summary

• The development of SALT readout ASIC for LHCb Upstream Tracker is almost completed.
  - Two 8-channel SALT prototypes, with almost complete functionality, were fabricated and tested
  - The 128-channel prototype was submitted in June:
    • chips were delivered at the end of August
    • waiting for the first test results...
  - Radiation tests are planned soon, first on 8-channels prototypes then full SALT
Thank You
SALT design
Single to Differential Converter (S2Diff)

- Pseudo-differential solution based on single-ended amplifiers
- Additional gain by 2 may be obtained in S2Diff
SALT Design Memory

• Challenge – packet size range: 1 byte (HEADER) – 100 bytes (NZS)

• Many RAM instances – the smaller RAM element the smaller area and power consumption

• Almost all input data goes directly to RAM – the rest waits in buffer

• Output circular buffer because variable number of e-links 3 – 6

Prepared for 12-bit based data packet
Tests of prototypes
Laser scan across strips

Pulse shape taken @

P-type ½ A sensor
Scan in 1 µm step
Deposition ~1 MIP

(~36) ~121 µm (~33)
(~190 µm)