14th Topical Seminar on Innovative Particle and Radiation Detectors (IPRD16)

3 - 6 October 2016

Siena, Italy

An ASIC for fast single photon counting in the LHCb RICH upgrade

C. Gotti

INFN and University of Milano Bicocca

on behalf of the LHCb RICH collaboration

The LHCb Experiment

- Single arm spectrometer at the LHC optimized for flavour physics
- Designed to detect particles produced at small angles w.r.t. beam
- Includes two Ring Imaging Cherenkov (RICH) detectors for p/K/ π separation, range 2-100 GeV/c

RICH1:

Acceptance 25-300 mrad

C_4F_{10} ($n=1.0014$): range 10-40 GeV/c

RICH2:

Acceptance 15-120 mrad

CF_4 ($n=1.0005$): range 15-100 GeV/c

LHCb RICH detectors

- Cherenkov photons are mirrored and focused onto the photodetector planes
- Need to detect single photons on $\approx \text{m}^2$ planes
- Pixel size $\approx 3 \times 3 \text{ mm}^2$

LHCb upgrade

- Planned to install in 2019-2020 to increase luminosity from 4 to 20 x 10³² cm⁻² s⁻¹
- The upgraded LHCb will use a triggerless readout at 40 MHz

LHCb RICH upgrade

- Overall detector structure unchanged
- Optical layout of RICH1 adjusted to keep the occupancy below $\approx 25\%$

Expected occupancy in the upgraded RICH1

LHCb RICH upgrade

- Multi-anode PMTs to be used as single photon sensors
- PMTs + front-end ASICs constitute the «elementary cells» (EC)

EC-R (2x2 small PMTs):

- 16x16 pixels of $\approx 3 \times 3 \text{ mm}^2$ size
- Qty: 480 (RICH1)
+ 192 (central RICH2)

EC-H (1 large PMT):

- 8×8 pixels of $\approx 6 \times 6 \text{ mm}^2$ size
- Qty: 384 (peripheral RICH2)

Multi-anode PMTs

Hamamatsu R13742

Based on the R11265
8x8 pixels in 1x1 inch²

Hamamatsu R13743

Based on the R12699
8 × 8 pixels in 2x2 inch²

- Average gain is $\approx 10^6$ at 1 kV
- Gain spread within a factor of ≈ 3 -4
- The pixel stray capacitance is low (≈ 1 pF)
- Transit time $\approx$ ns
- The single photon spectrum is clearly separated from the noise pedestal

The Elementary Cell

- Designed to minimize stray capacitance at the input (lower noise and crosstalk)
- Requires a front-end ASIC with a low number of channels and low power consumption

The Elementary Cell

Digital board

Acquires digital signals from the CLARO outputs
2 DBs read out 4 elementary cells

Readout architecture

Main requirements for the readout chain:

- Able to sustain rates up to ≈ 40 MHz per pixel (25% occupancy in the hottest regions)
- Low power consumption (closely packed channels)
- Radiation tolerant up to ≈ 10 kGy (1 Mrad) TID and 10^{13} (n,p) cm^{-2} hadron fluences (includes safety factor of ≈ 5)

Front-end ASIC + FPGA architecture results in:

- Separation of analog and digital domain to choose the best technology for each
- No noisy clock signals in the front-end ASIC (easier to design)
- The digital functionalities in the FPGA can be reprogrammed after deployment

The CLARO8 ASIC

- 4- channel prototype «CLARO-CMOS» designed in 2011
- 8-channel version «CLARO8» designed in 2014, improved versions in 2015 and 2016
- Power consumption < 1 mW / channel in idle, < 2.5 mW / channel at high rate (30 pF output loads)
- 0.35 um CMOS technology (Austria Micro Systems) is relatively inexpensive
- 128-bit configuration register with triple modular redundancy and SEU counter, synthesised with RHBD digital cells designed at IMSE-CNM Sevilla

8 outputs

128-bit config register with TMR

Analog channels

8 inputs

The CLARO8

In each channel:

- 4 gain settings (1, 1/2, 1/4, 1/8)
- 64 comparator thresholds (threshold step $\approx 30 \text{ ke}^-$ (5 fC) at attenuation 1)
- 640 fF calibration capacitor to inject test signals at the input
- Recovery time $< 25 \text{ ns}$ for single photon signals (10^6 e^-) allows to count at 40 MHz without dead time

The CLARO8

Channel specifications for 10 pF input load, 30 pF output load:

Power consumption (low rate)		< 1 mW/channel
Power consumption (high rate, 10^7 hits/s)		< 2.5 mW/channel
Input noise	(typ: 4 ke ⁻ RMS)	< 10 ke ⁻ RMS
Input impedance (low frequency)		< 100 Ω
Input impedance (high frequency)		< 1 k Ω
Amp gain settings		1, 1/2, 1/4, 1/8
Amp dynamic range at gain 1 [1/8]		5 Me ⁻ [40 Me ⁻]
Amp peaking time	(typ: 7 ns)	< 10 ns
Amp recovery (typical signals)		< 25 ns
Amp recovery (from saturation)		< 50 ns
Comparator delay		< 10 ns
Comparator recovery	(typ: 6 ns)	< 25 ns
Threshold settings at gain 1 [1/8]		64 steps $\times$ 30 ke ⁻ [240 ke ⁻]
Threshold range at gain 1 [1/8]		0 $\div$ 2 Me ⁻ [16 Me ⁻]

Typical single photon hit (10^6 e⁻)
at the output of the CLARO

Test beam results

- Test beams performed at the CERN North Area with a π beam at 180 GeV/c
- Glass lens as a solid focusing radiator
- Operation of 4 near-final elementary cells
- Test of hardware, software, mechanics, cooling...

Test beam results

- About 30 photoelectrons detected in average for each track
- Cherenkov radius ≈ 60 mm
- Number of photons and Cherenkov radius agree with simulations
- Resolution ≈ 0.5 mm (pixel size)
- Crosstalk below 1%

Summary and future plans

The front-end designed for the LHCb RICH upgrade:

- Allows fast counting of single photons (up to 40 MHz)
- Is engineered to cover large planes with small dead area, low noise and low crosstalk
- Withstands radiation up to the levels required (≈ 10 kGy (1 Mrad) TID and 10^{13} n,p cm⁻²)

All the elements are reaching the production phase:

- Test beam in autumn with final prototypes
- Production of 40'000 CLARO ASIC will start in early 2017

The LHCb RICH upgrade is on track for installation in LS2 (2019-2020)...

Thanks!

Signals

- Very good performance on the test bench
- The recovery time is less than 25 ns
- The static power consumption is 0.75 mW per channel
- At 10 MHz hit rate with a 10 pF output load the power consumption increases to 1.4 mW per channel

CLARO with SiPMs

- The 4-channel prototype was also tested with SiPMs
- Activity related with the SuperB IFR detector in Ferrara
- Signals are slower than nominal due to large input capacitance $\approx 50\text{-}150\text{ pF}$
- Tested with $1 \times 1\text{ mm}^2$ and $3 \times 3\text{ mm}^2$ SiPMs
- With 1 mm^2 devices the various peaks (2-10 photoelectrons) are clearly separated

Timing

- The timing performance of the 4-channel prototype was measured on the test bench
- The time walk is ≈ 3 ns (or ≈ 1.5 ns if power is increased to 1.5 mW/channel)
- Jitter on the rising edge is ≈ 100 ps on threshold, decreasing to 10 ps for larger signals
- Tests of the CLARO with a MCP-PMT are planned

Spread

Pre-production run of 220 CLARO8 chips in 2015

- The average threshold at code 15 is 495 ke- $\rightarrow$ Average step is ≈ 33 ke-
- The total threshold spread between channels is 71 ke- $\rightarrow \sigma \approx 2$ threshold steps ($\rightarrow 15\%$)
- No correlation between channels in the same chip
- The CLARO8 gain/threshold spread can be calibrated away